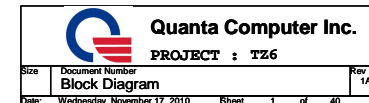





**LAYER 1 : TOP**  
**LAYER 2 : GND1**  
**LAYER 3 : IN1**  
**LAYER 4 : VCC**  
**LAYER 5 : IN2**  
**LAYER 6 : IN3**  
**LAYER 7 : GND2**  
**LAYER 8 : BOT**



## Table of Contents

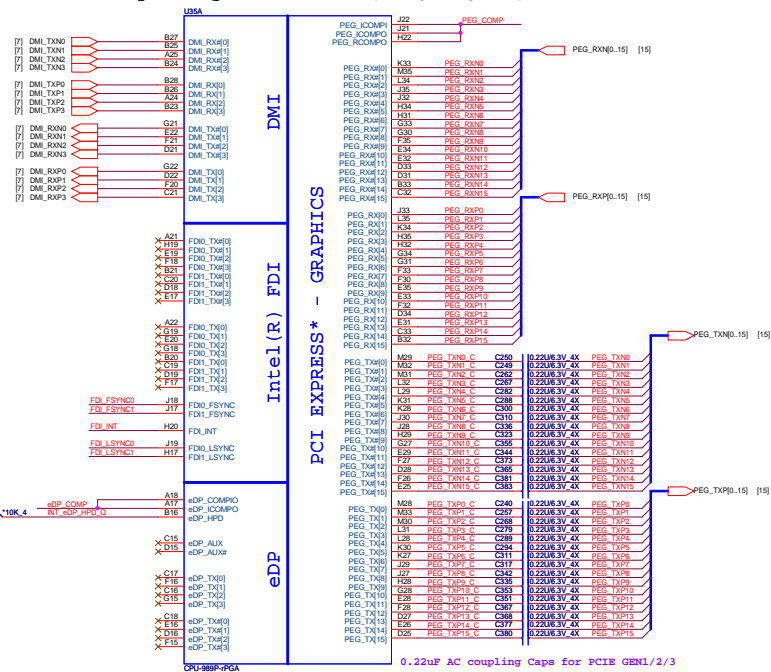
PAGE	DESCRIPTION	BOI-FUNCTIONS
1	Schematic Block Diagram	
2	Front Page	
3-6	Processor	CPU
7-12	PCH	CLG
8	RTC	RTC
13-14	DDRIII SO-DIMM	DDR
15	VGA Connector	VGA
16	LCD Panel	LDS
	CRT	CRT
	CCD	CCD
	HALL SENSOR&BACK LIGHT SWITCH	HSR
17	HDMI comm part	HDM
18	SATA ODD	ODD
	Main SATA HDD & 2nd SATA HDD	HDD
	G-Sensor	H3D
19	5 IN 1 Card reader	MMC
	IEEE1394	FIW
20	MINI Card (Wi-Fi)	WLN
	MINI Card 2nd	MNC
21	INT KeyBoard & K/B LED Power	KBC
	LED Board	LED
	TP&FP board	TPD,FPD
	Bluetooth Connector	BTM
	MMB Connector	MMB
	Power SW	PSW
22	New Card (Express Card)	EXC
	E-SATA comb USB	ESA
	USB Connector	USB
	Audio & USB Board	USB,ADO
	Satellite LED	LED
	RF LED / WIMAX LED / Kill SW	KSW
23	EC WP8763LDG/WPC8769L(O)	KBC
		CIR
24	Codec (CX20583)	ADO
25	HOLE	
26	Atheros LAN	LAN
27	NVRAM Connecytor	NVR
28	Charger (ISL6251A)	PWM
29	System 5V/3V (RT8210B)	PWM
30	CPU CORE (MAX17511)	PWM

POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
VIN	10V~+19V		S0~S5
+VCCRTC	+3.0V~+3.3V		S0~S5
+3V	+3.3V	MAIN_ON	S0
+3V_S5	+3.3V	S5_ON	S0~S5
+3V_HDP	+3.3V	MAIN_ON	S0
+3VPCU	+3.3V	AC/DC Insert enable	S0
+5V	+5V	MAIN_ON	S0
+5V_S5	+5V	S5_ON	S0~S5
+5VPCU	+5V	AC/DC Insert enable	S0~S5
+1.8V	+1.8V	MAIN_ON	S0
+1.5V	+1.5V	MAIN_ON	S0
+1.5V_S5	+1.5V	S5_ON	S0~S5
+1.5V_SUS	+1.5V	SUSON	S0~S3
+VCC_CORE		VRON	S0
+VTT	+1.05V	MAIN_ON	S0
+1.05V	+1.05V	MAIN_ON	S0

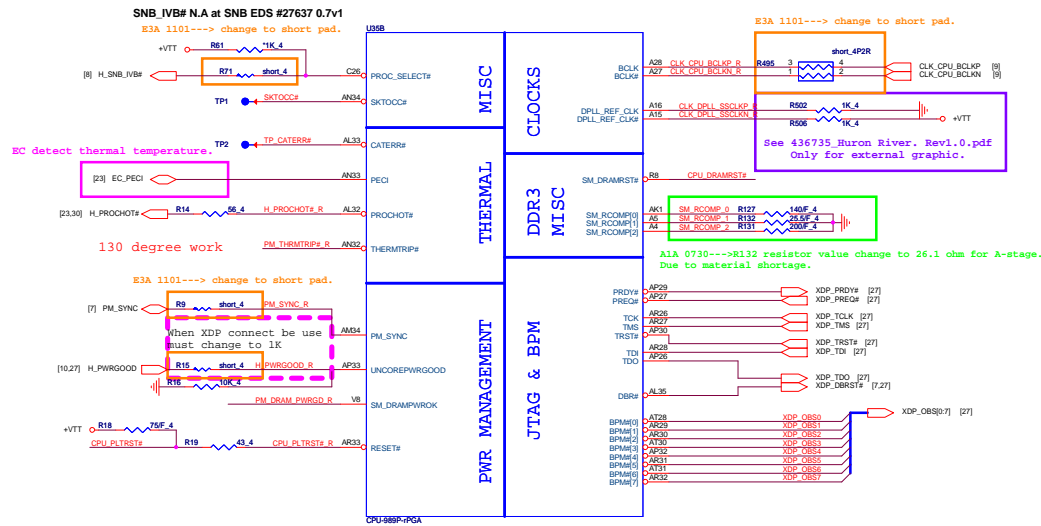
GND PLANE	PAGE
 CARD_GND	19
 AGND_DC/DC	24
 GND	ALL

PAGE	DESCRIPTION	BOI-FUNCTIONS
31	+VTT (RT8202A)	PWM
32	+1.05V (RT8202A)	PWM
33	+VCCSA(ISL95870A)	PWM
34	DDR 1.5V (RT8207L)	PWM
35	Discharge (1.5V_S5/1.8V)	PWM
36	Power Tree Table	

## Sandy Bridge Processor (DMI,PEG,FDI)



## Sandy Bridge Processor (CLK,MISC,JTAG)



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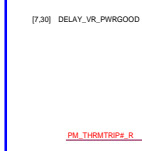
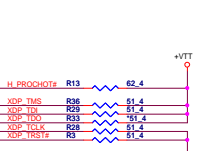
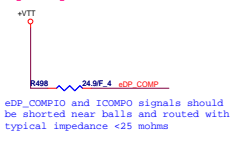
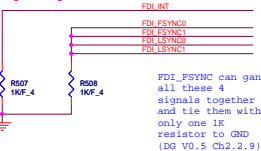
## FDI Disabling (Discrete Only) [CPU]

## DP &amp; PEG Compensation [CPU]

## Processor pull-up(CPU) [CPU]

## Level Shift [CPU]

## Thermal Trip [CPU]



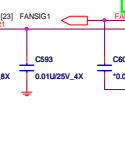
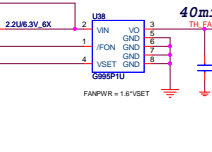
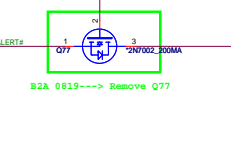
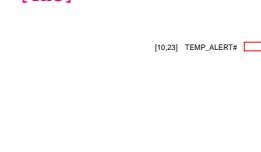
## CPU FAN CTRL [THC]

## 3mA(40mils)

## 40mils

## B2A 0817----&gt; Remove R587

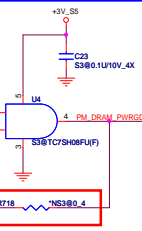
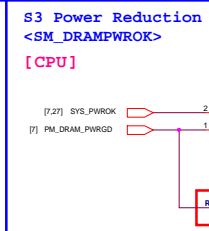
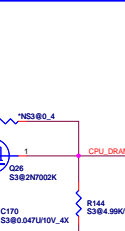
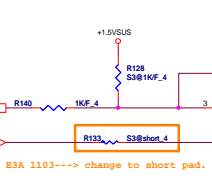
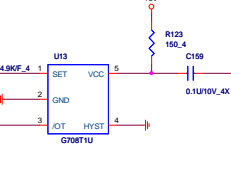
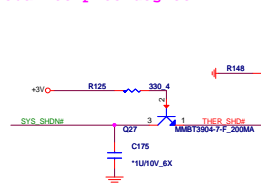
## B2A 0817----&gt; change to short pad.



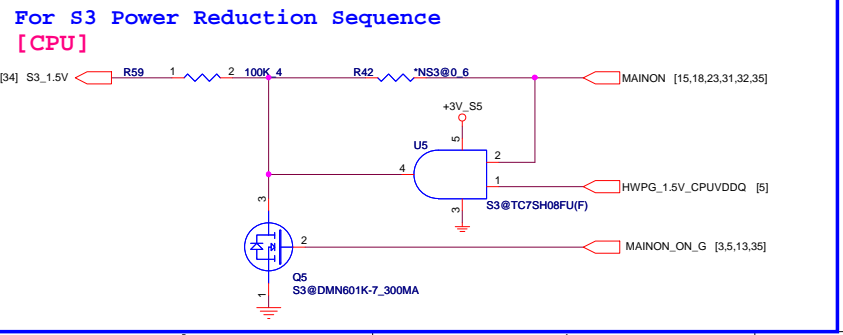
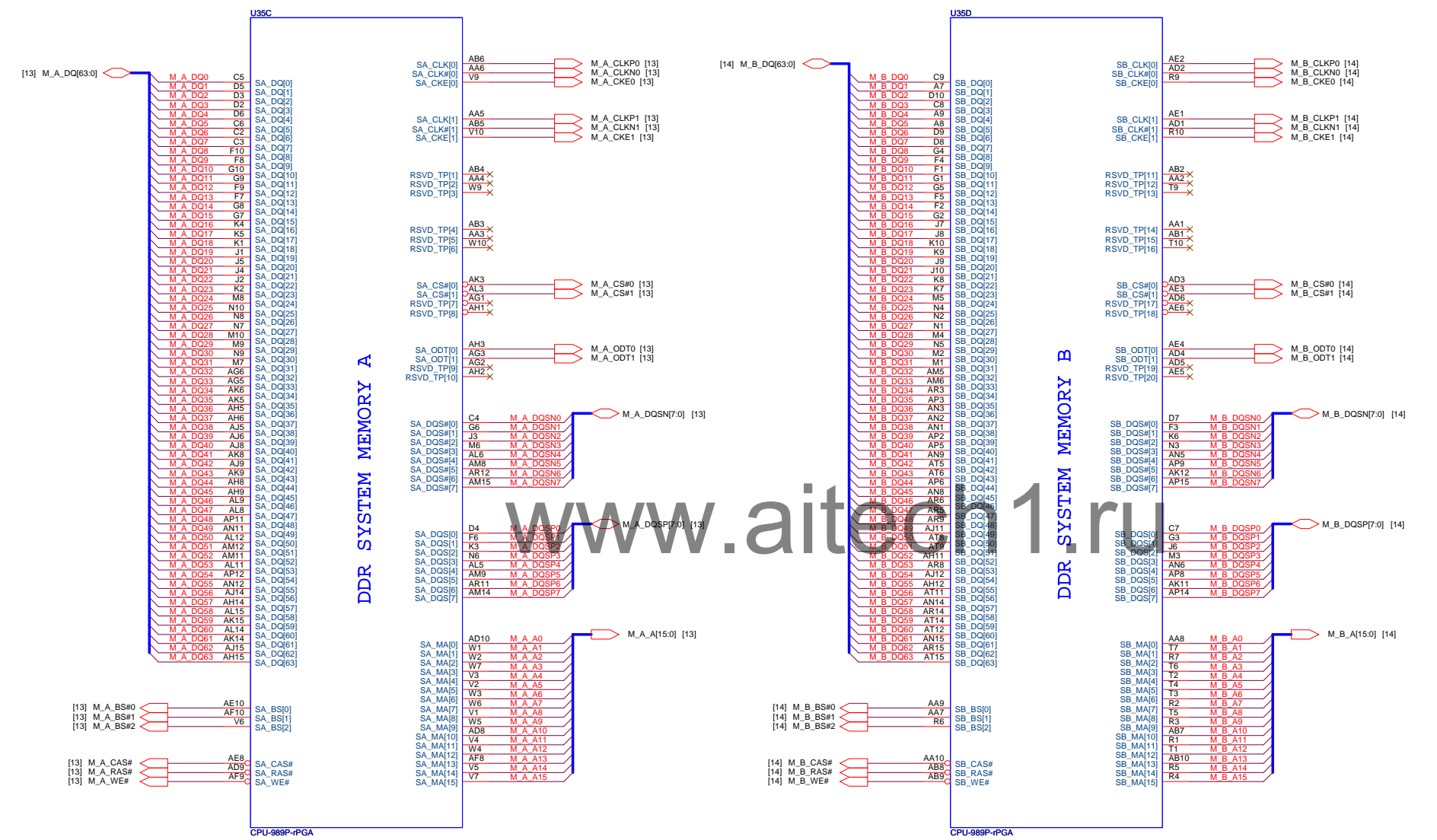
## CPU Thermal monitor [THC] Local temp 85 degree

## S3 Power Reduction &lt;SM\_DRAMRST#&gt; [CPU]

## S3 Power Reduction &lt;SM\_DRAMPWRK#&gt; [CPU]

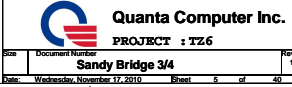


Sandy Bridge Processor (DDR3)

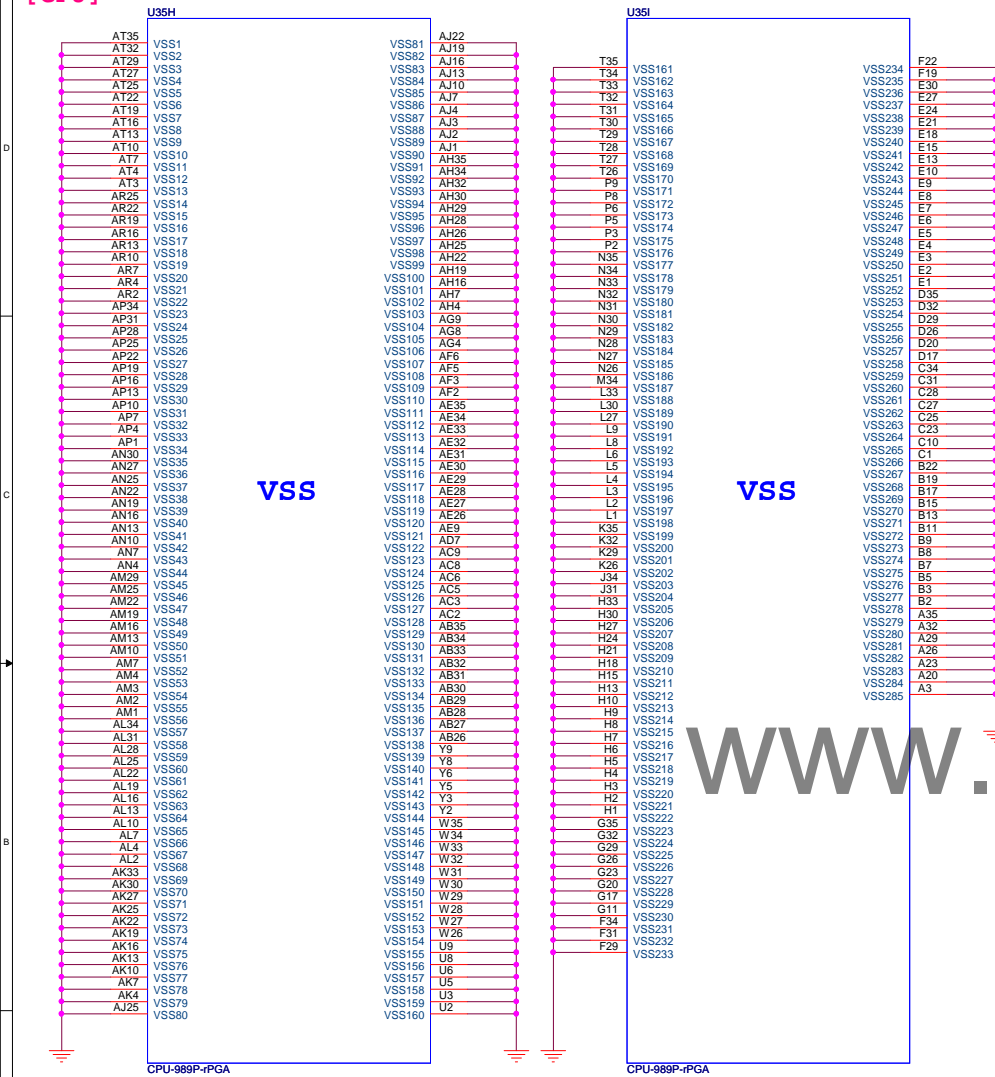




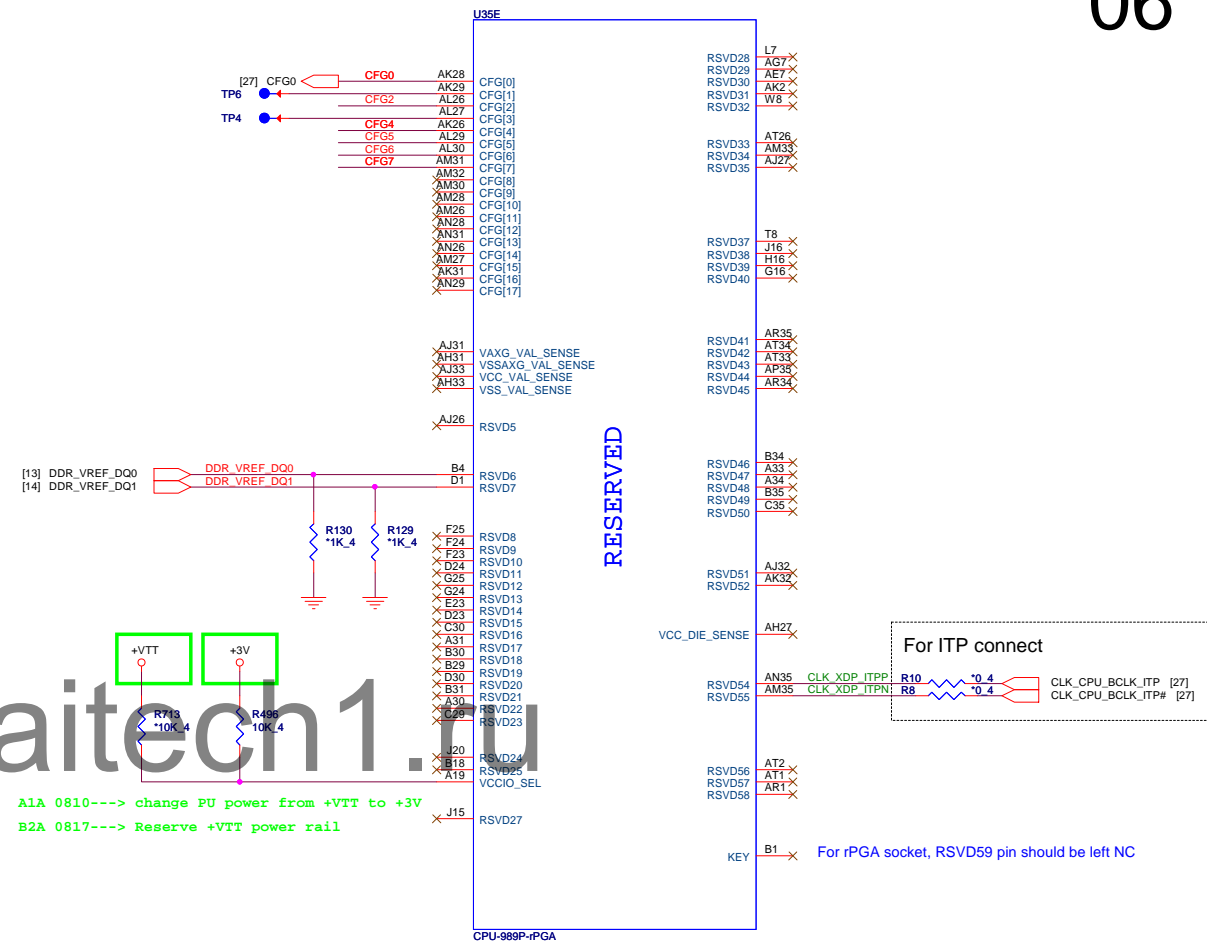
Sandy Bridge Processor (GRAPHIC POWER)



Sandy Bridge Processor (GND)



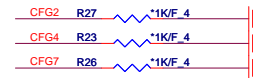
Sandy Bridge Processor (RESERVED, CFG)



## Processor Strapping

**The CFG signals have a default value of '1' if not terminated on the board.**

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



CFG[6:5] (PCIE Port Bifurcation Straps)

```
11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled
```

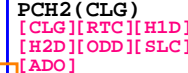
**Quanta Computer Inc.**

PROJECT : TZ6

Size	Document Number	Rev
	<b>Sandy Bridge 4/4</b>	1A
Date:	Wednesday, November 17, 2010	Sheet 6 of 40



## 08



ACZ\_SYNC\_R1

3V\_RTCO

R363  
33K/F\_4

Q51  
2N7000

C406  
33050V\_4N

C400  
18P50V\_4C

R862  
short\_4

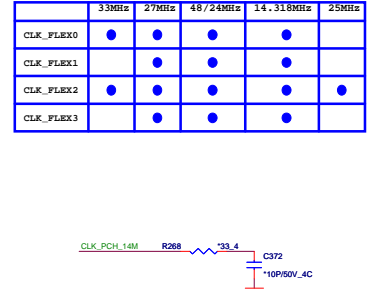
E3A 1103--> change to short pad.




## U41B

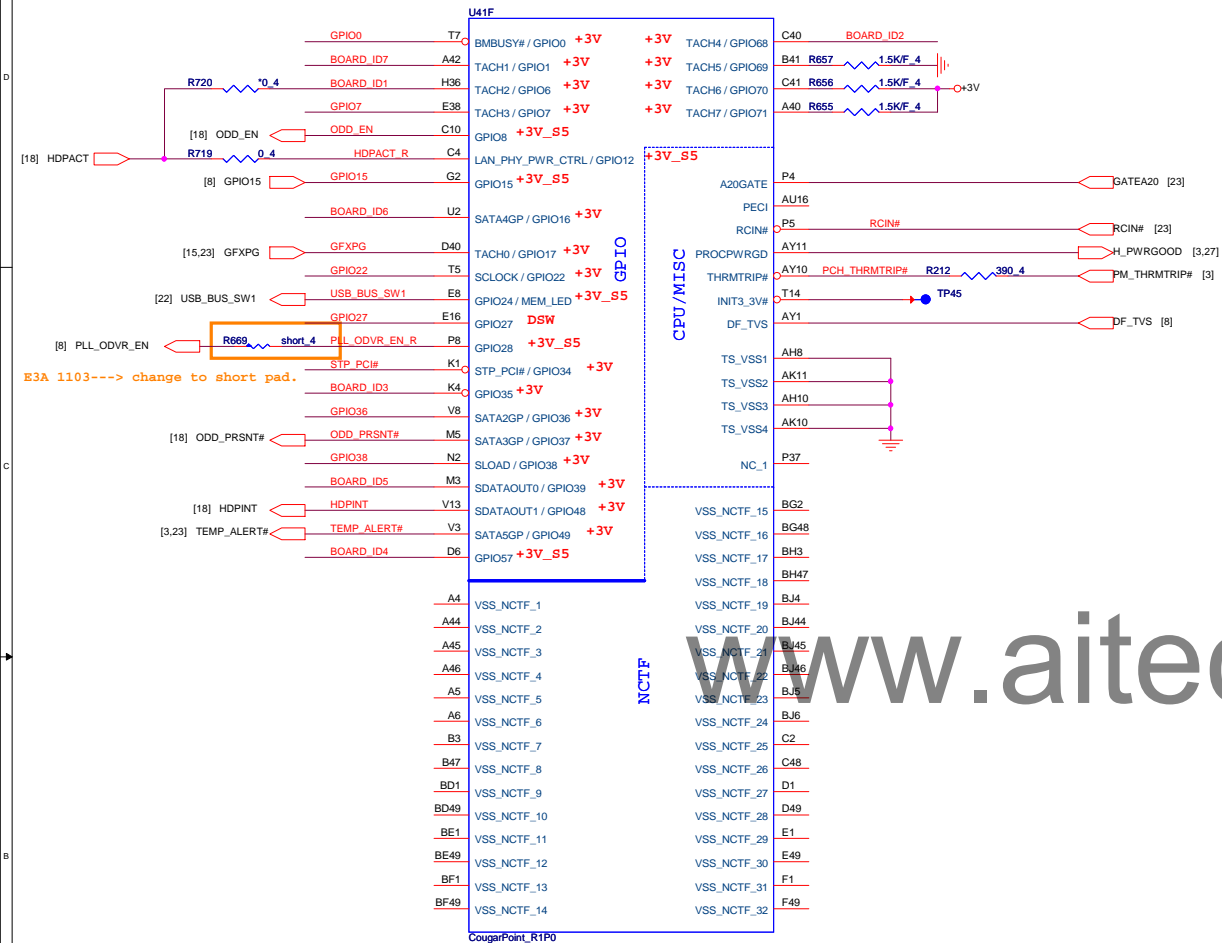


## [ CLG ]



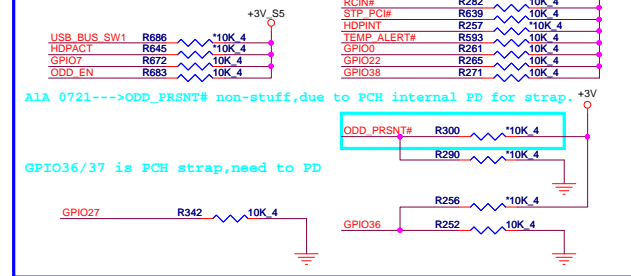
 <b>Quanta Computer Inc.</b> <b>PROJECT : TZ6</b>	
Size	Document Number
<b>Cougar Point 3/6</b>	
Date: Wednesday, November 17, 2010	Sheet 9 of 40

## Cougar Point (GPIO,VSS\_NCTF,RSVD)

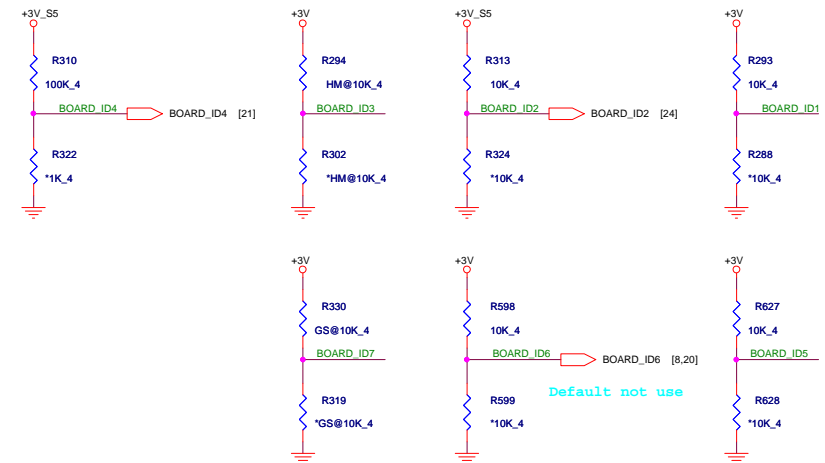


## GPIO Pull-up/Pull-down(CLG)

[CLG]



Board ID	ID7	ID6	ID5	ID4	ID3	ID2	ID1
Reserve							H L
W/ HK SPKR W/ Normal SPK						H L	
W/ HDMI W/O HDMI					H L		
W/O LED KB W/ LED KB				H L			
Reserve							
Reserve							
W/ G-SENSOR W/O G-SENSOR	H L						



Quanta Computer Inc.

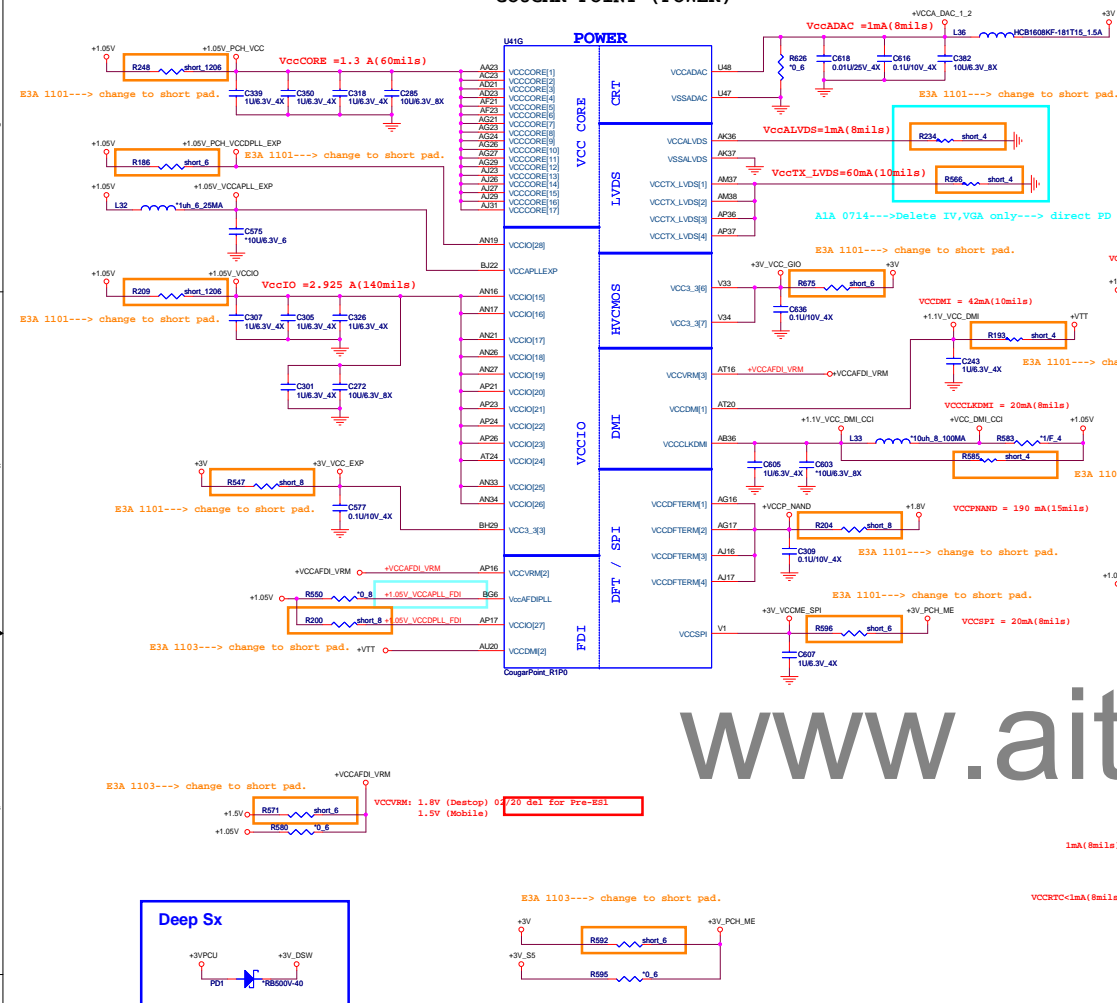
PROJECT : T26

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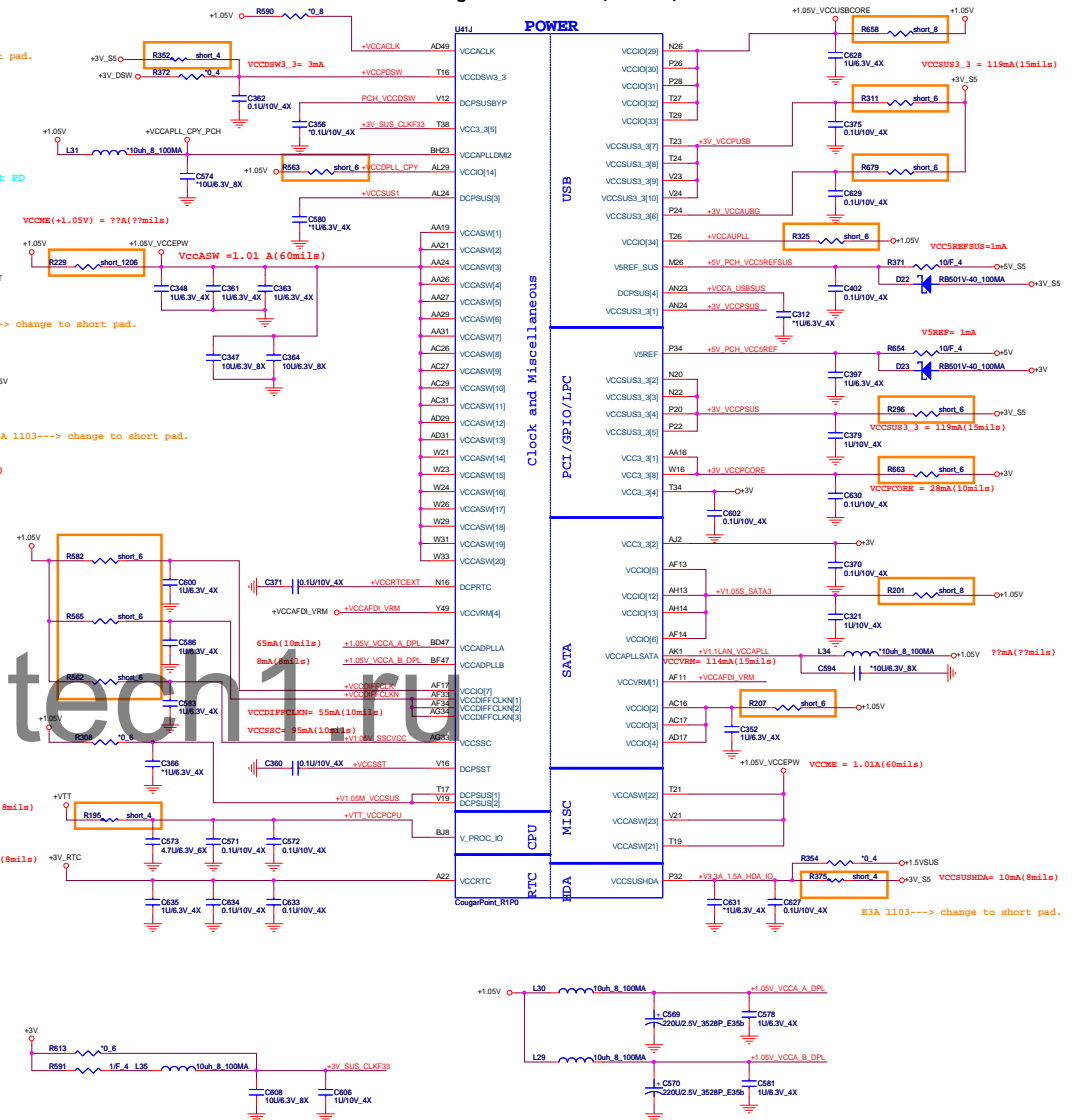
Date: Wednesday, November 17, 2010	Sheet 10 of 40
------------------------------------	----------------



## COUGAR POINT (POWER)

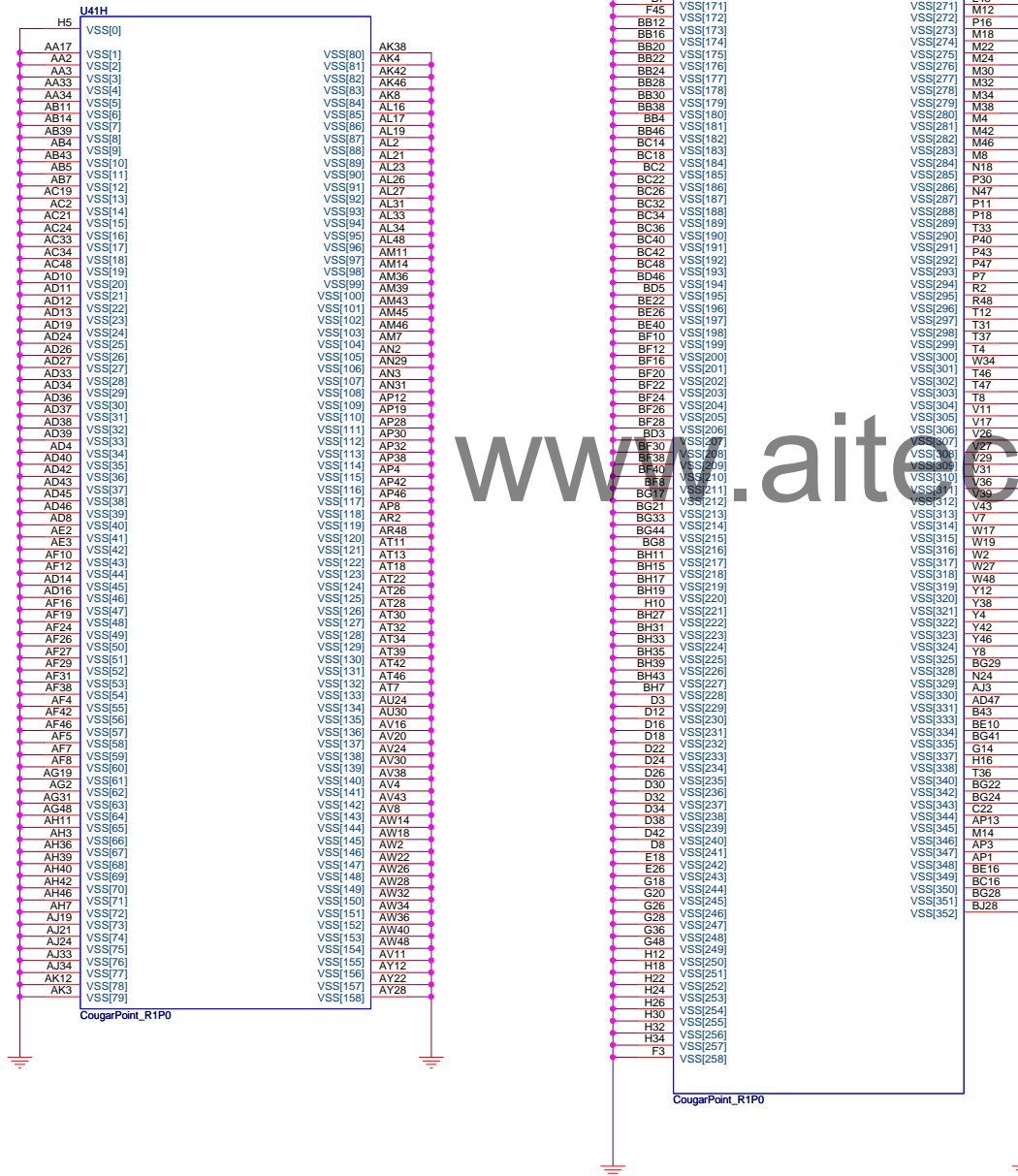


Cougar Point-M (POWER)





## IBEX PEAK-M (GND)

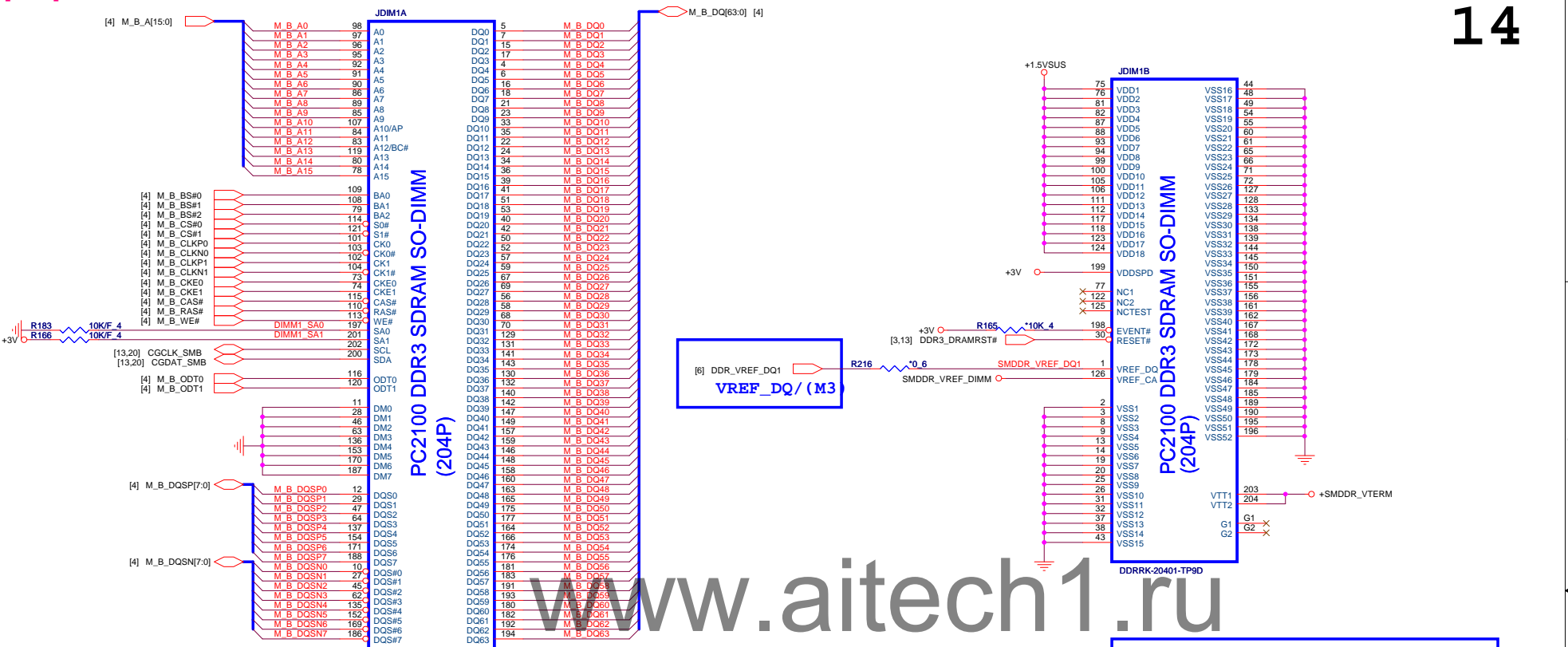


Quanta Computer Inc.

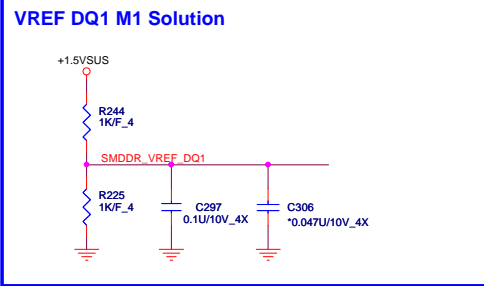
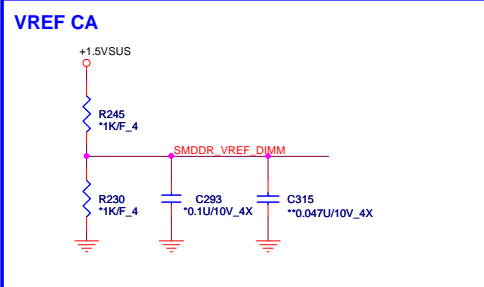
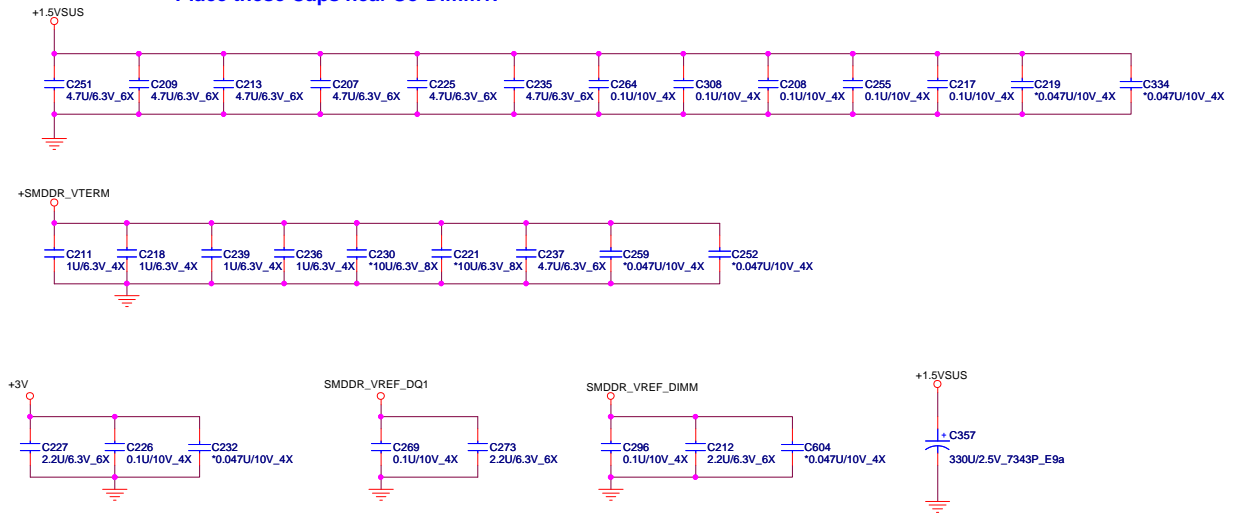
PROJECT : TZ6

Size	Document Number	Rev
	Cougar Point 6/6	1A
Date:	Wednesday, November 17, 2010	Sheet 12 of 40

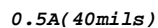
Rev  
1/Rev  
1/Rev  
1/Rev  
1/Rev  
1/Rev  
1/



Place these Caps near So-Dimm1.



[VGA]



1.5A(80mils)

15

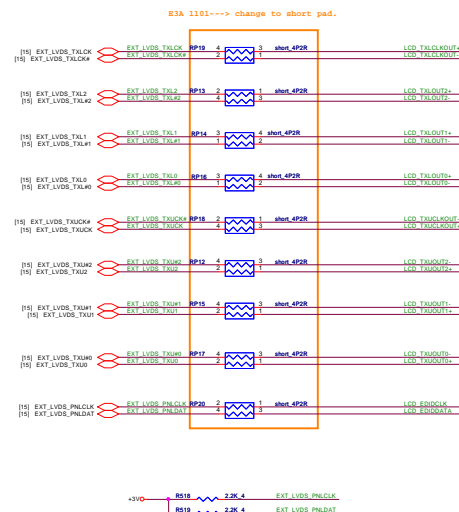


8.5A(400mils)

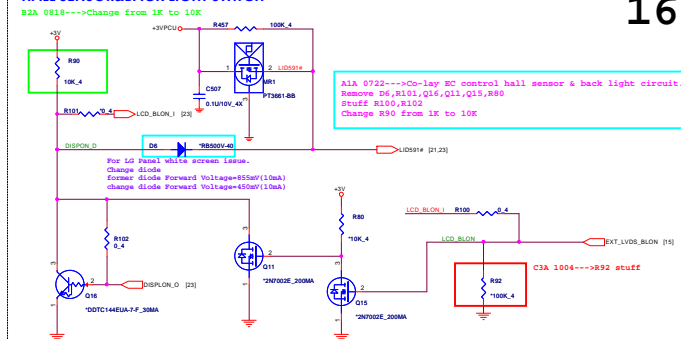


[THV]

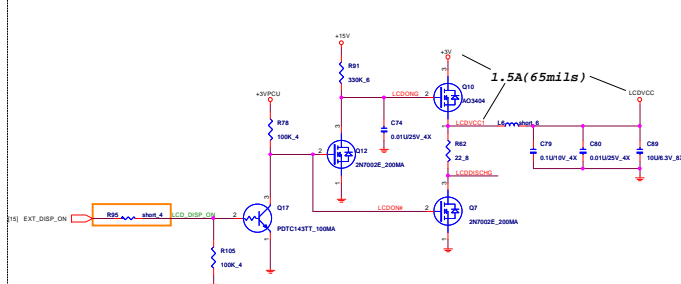




**HALL SENSOR&BACK LIGHT SWITCH [HSR]**

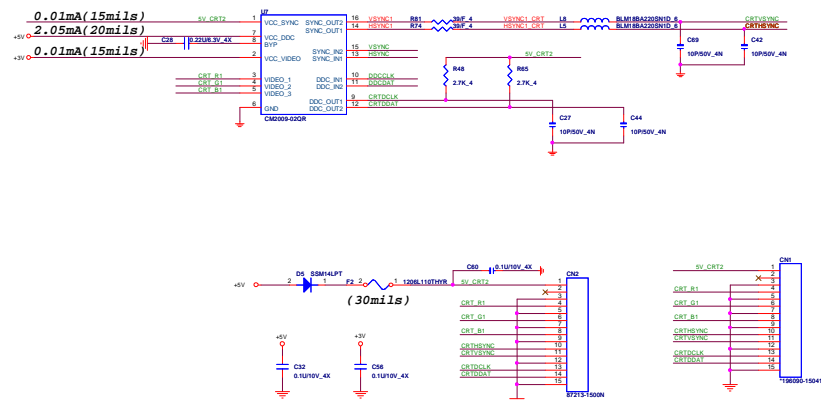
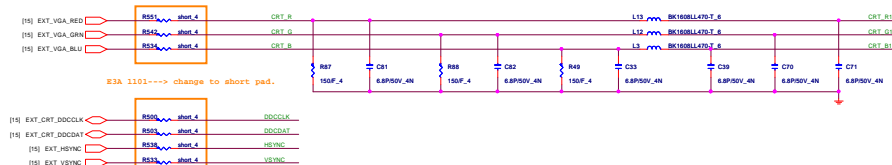


LCD POWER SWITCH [LDS]



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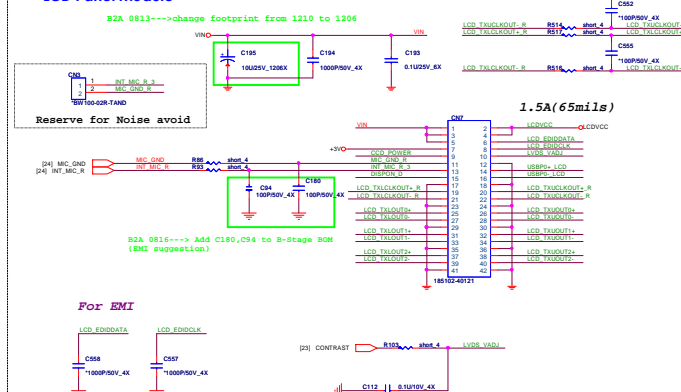
CRT [CRT]

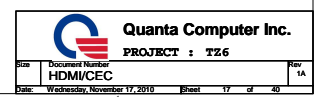
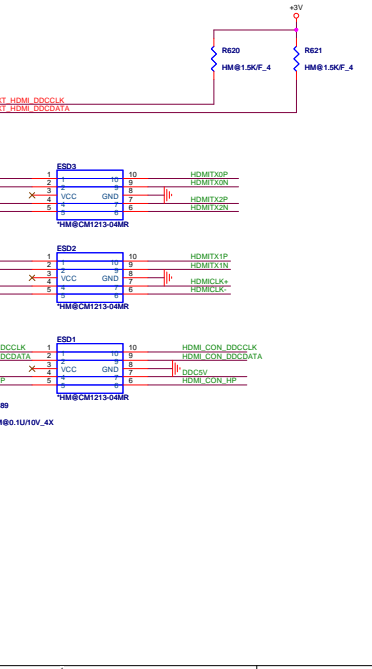
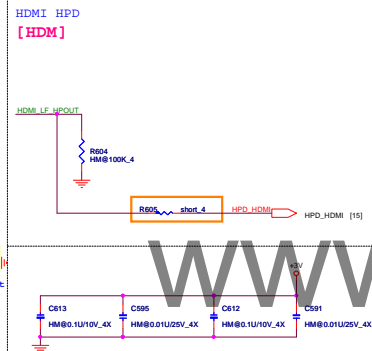
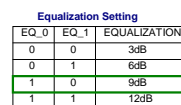


CCD  
[ CCD ]

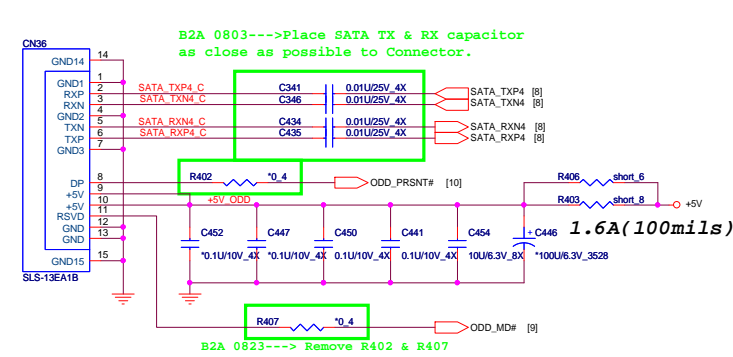


LCD Panel Module [LDS]

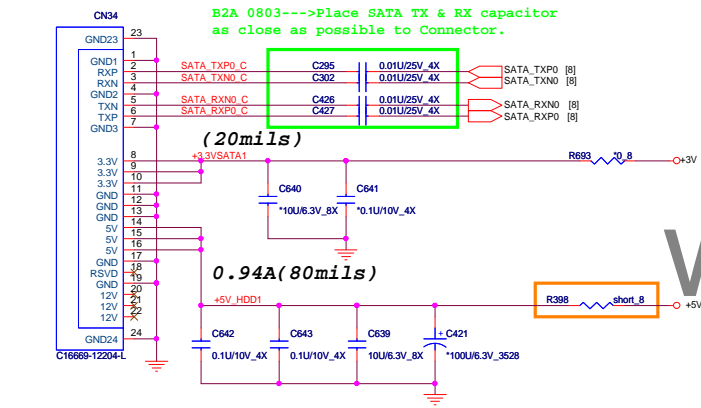




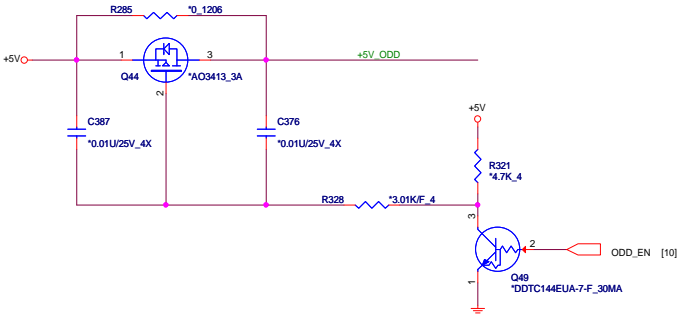
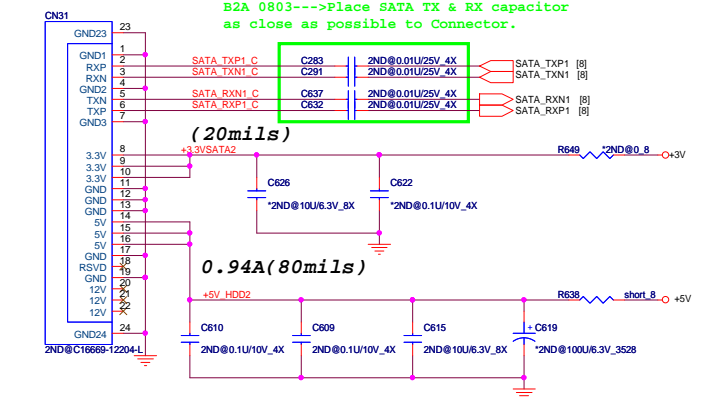
SATA ODD  
[ODD]



Main SATA HDD  
[H1D]



2nd SATA HDD [H2D]



FS (Full Scale) selection

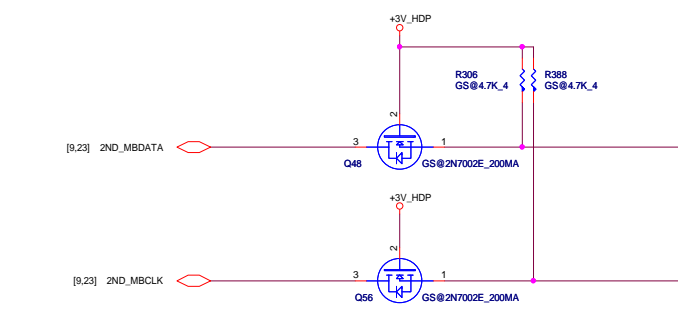
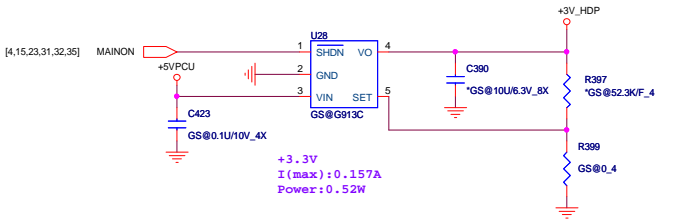
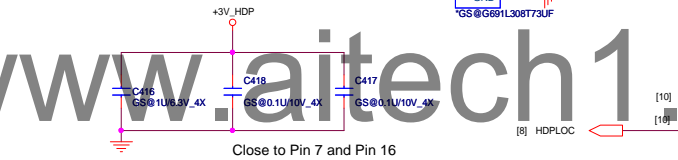
FS	0	1
2g Full-Scale		6g Full-Scale

PD (Power Down) selection

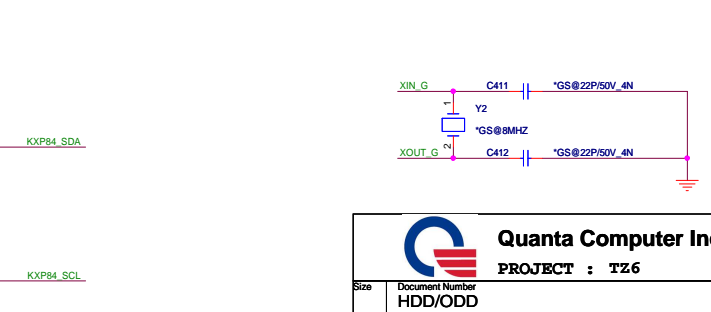
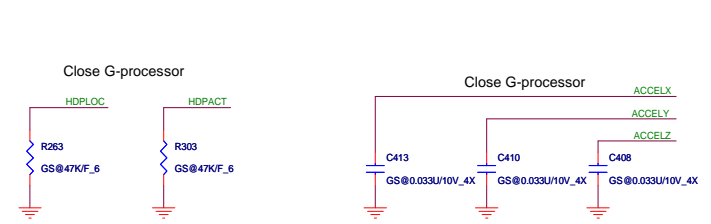
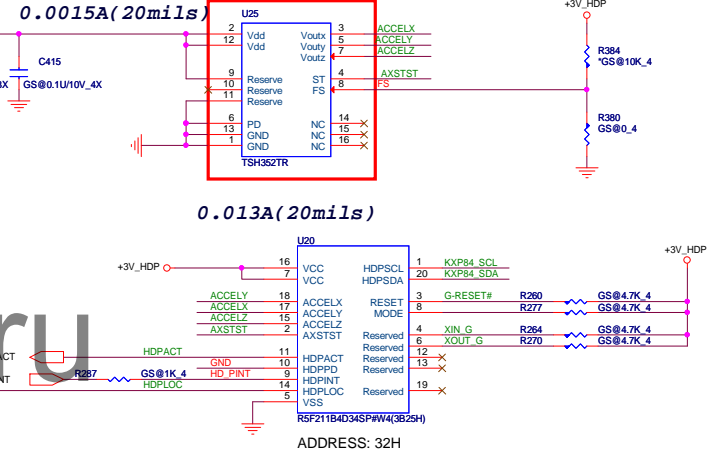
PD	0	1
Normal Mode		Power-down mode

HDPPD selection

HDPPD	0	1
Normal Mode		Power-down mode



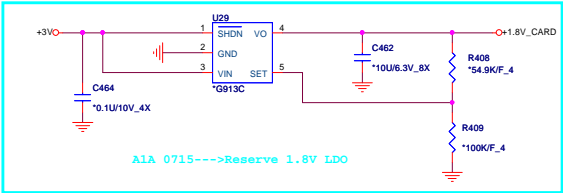
G-sensor  
[GSR]



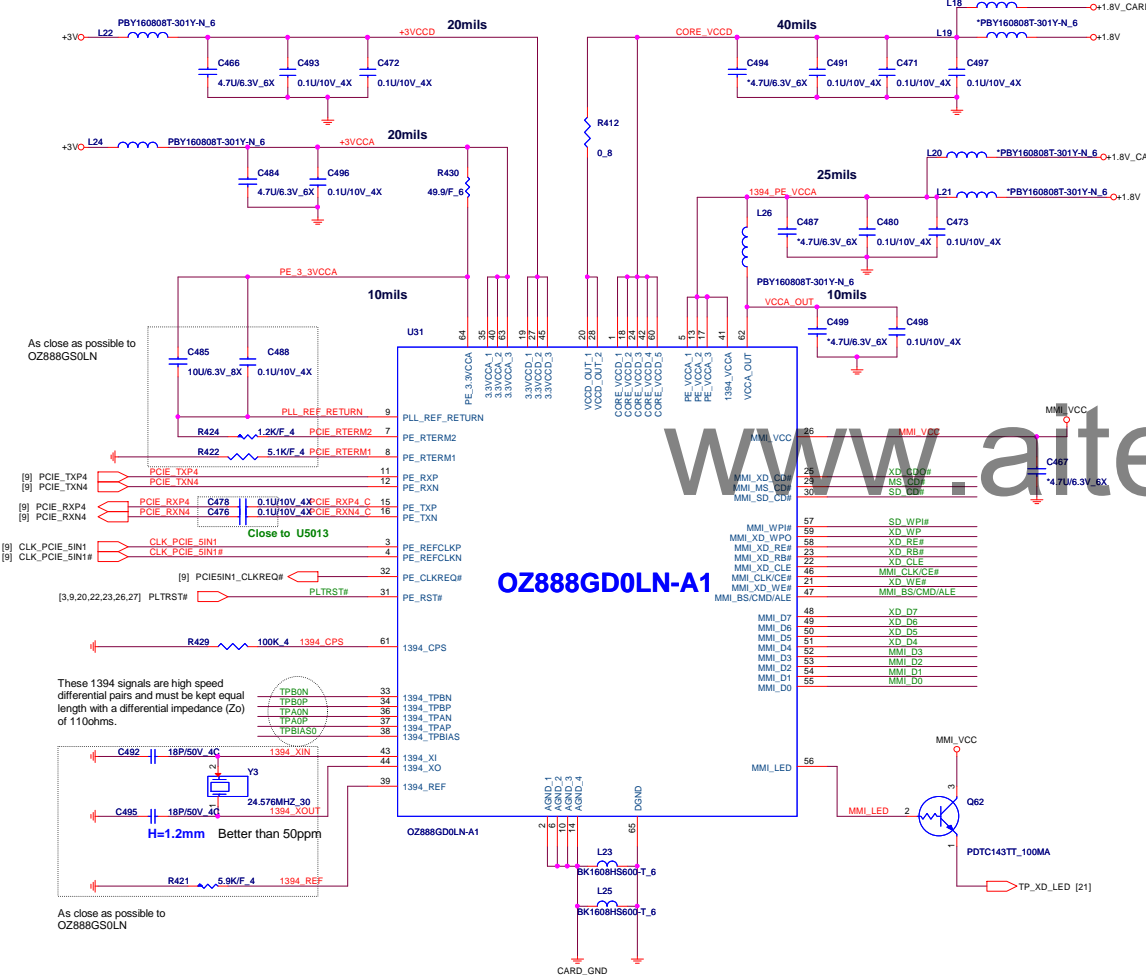


OZ888GD0LN-A1  
[MMC][FIW]

$V_{out}=1.25[1+(52.3/100)]=1.903V$   
 $V_{out}=1.25[1+(54.9/100)]=1.936V$

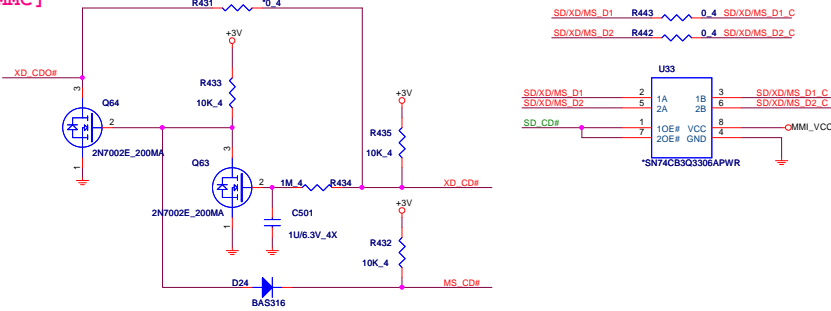


Each power pin is 100mA



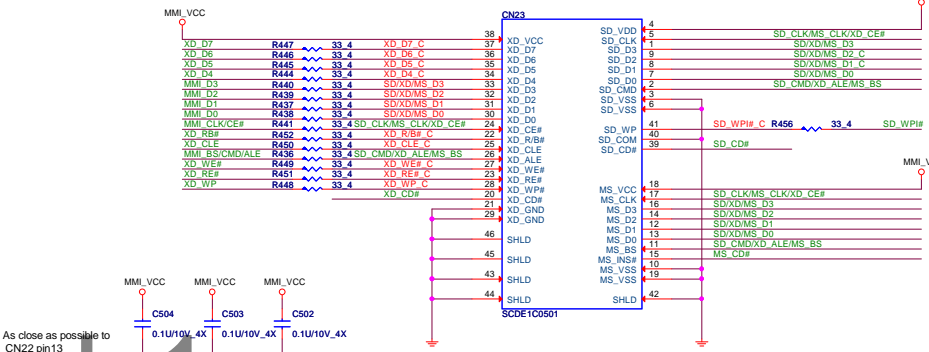
OZ888GD0LN-A1

[MMC]



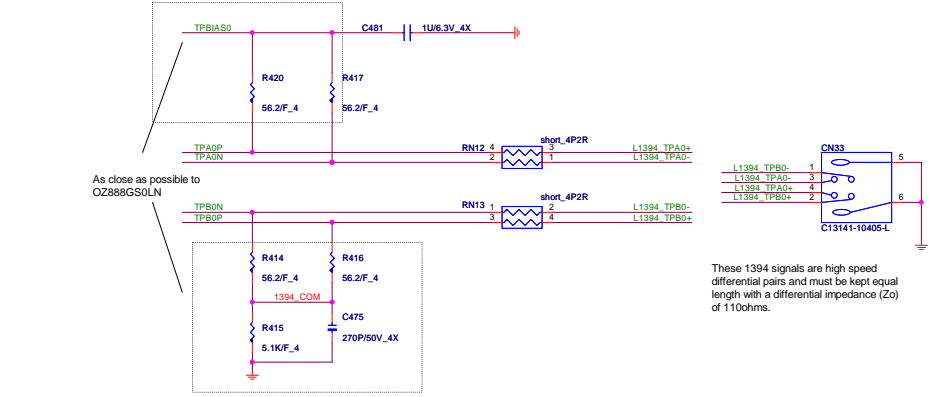
5 IN 1 CARD READER

[MMC]



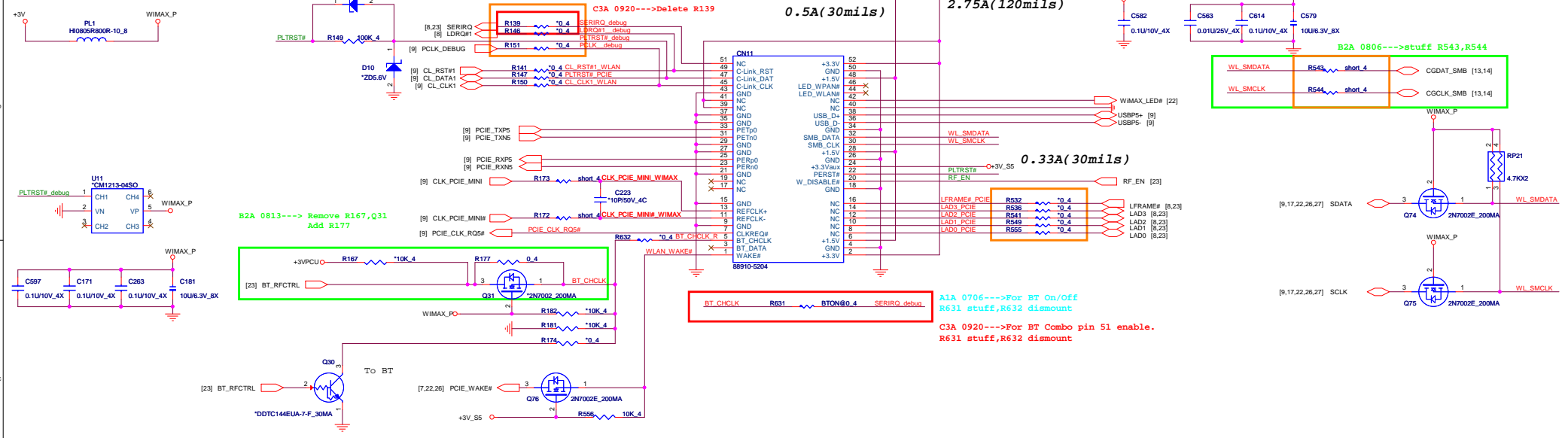
As close as possible to CN22 pin13

1394  
[FIW]

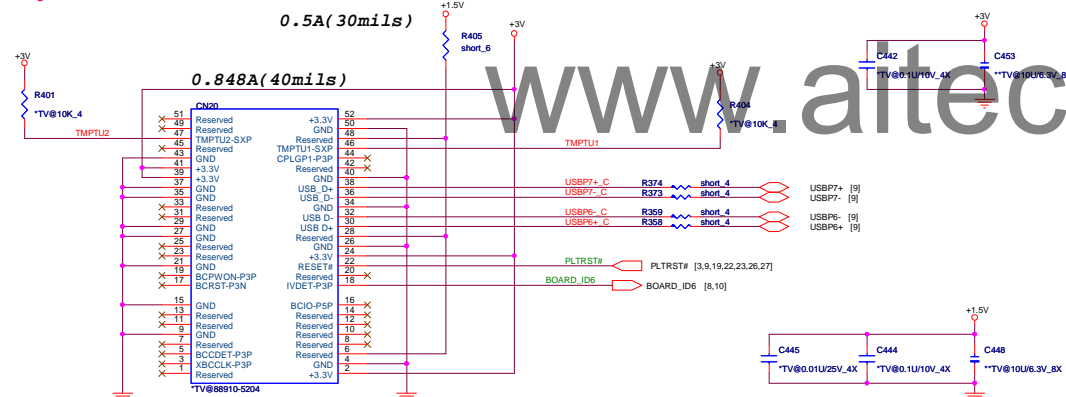


These 1394 signals are high speed differential pairs and must be kept equal length with a differential impedance (Zo) of 110ohms.

```
MINI Card Slot#1 [MNW][BTM]
(WiFi)
```

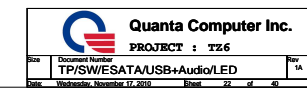
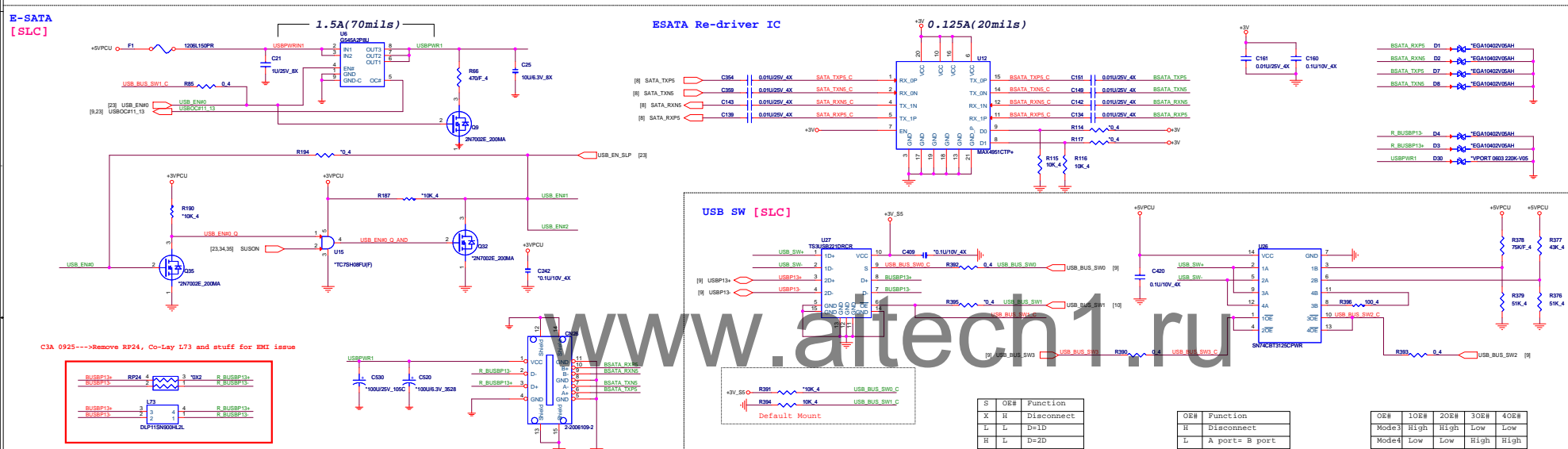


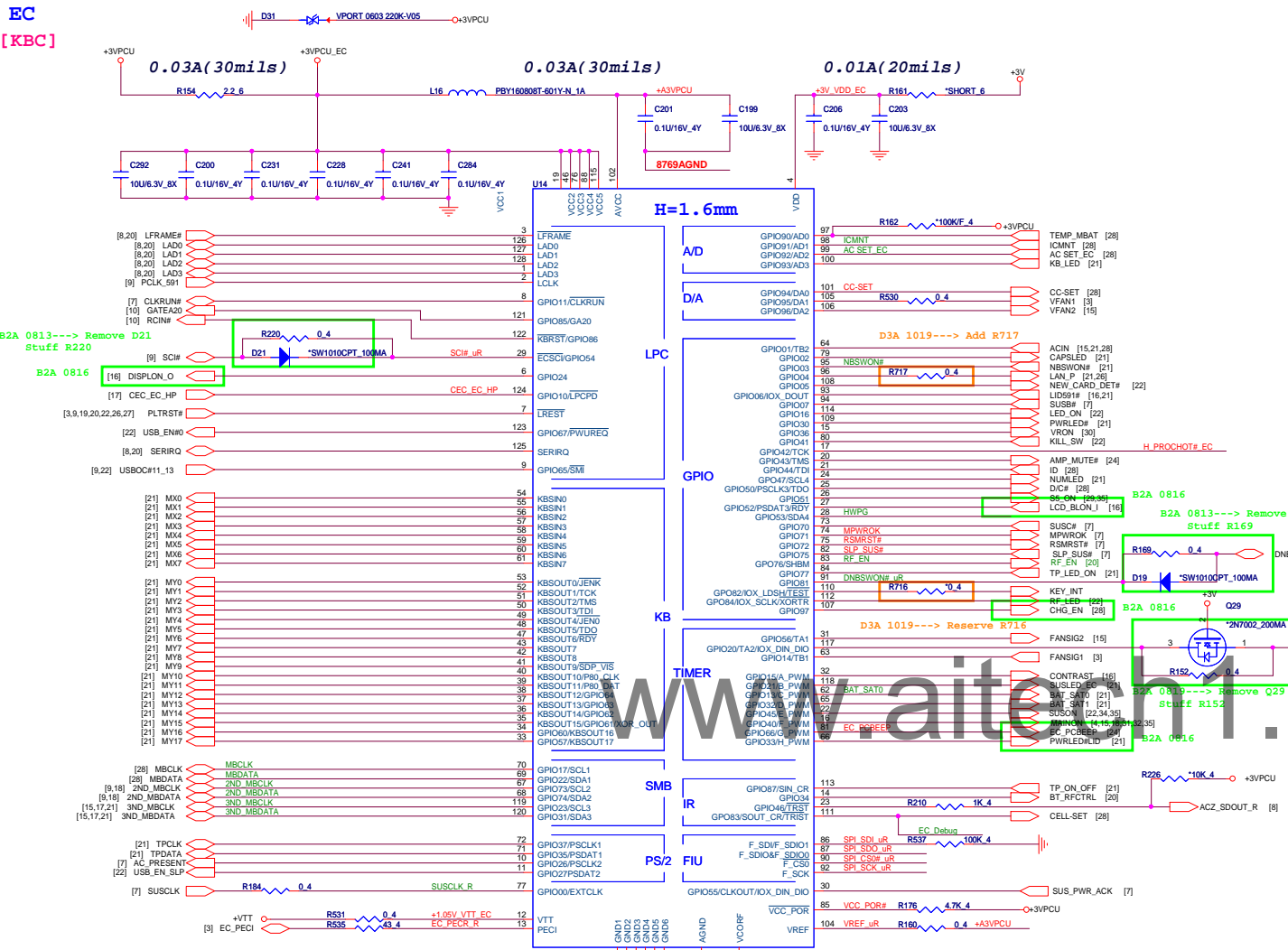
MINI Card Slot#2 [MNT]  
(TV Tuner)



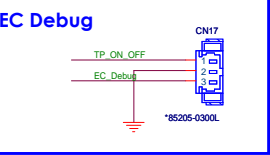
PCIE Mini Slot H=4	
Slot#1	WiFi
Slot#2	TV Tuner

[illegible][illegible][illegible]



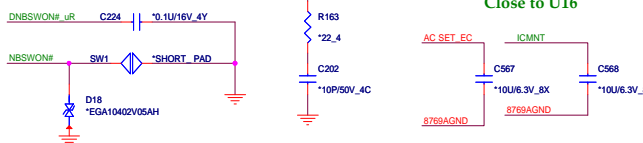


## EC Debug

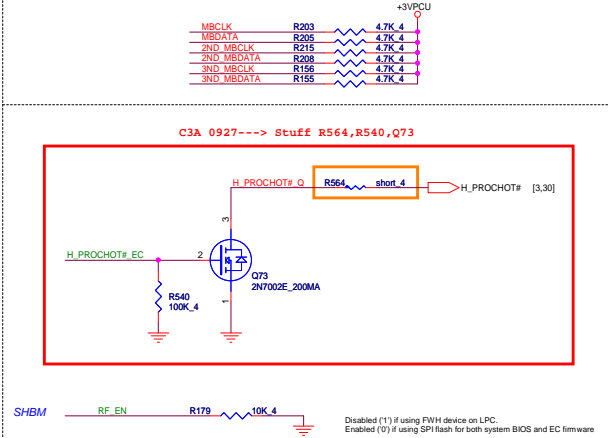


### SMBUS Table

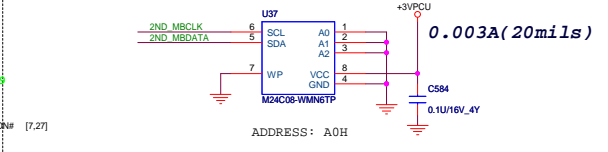
SMBUS	Devices	Address
1	Battery	16H
2	PCH SML1	N/A
	3D Sensor	32H
	EC EEPROM	A0H
3	VGA Board Thermal Sensor	98H
	Touch Sensor	58H
	HDMI CEC	34H



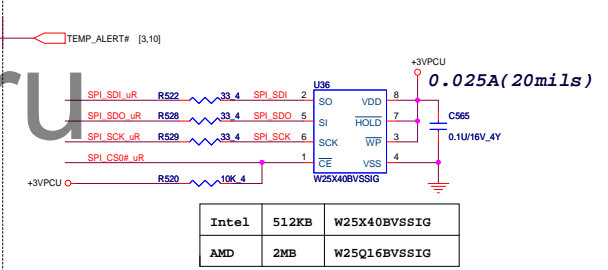
## SM BUS PU



## ID



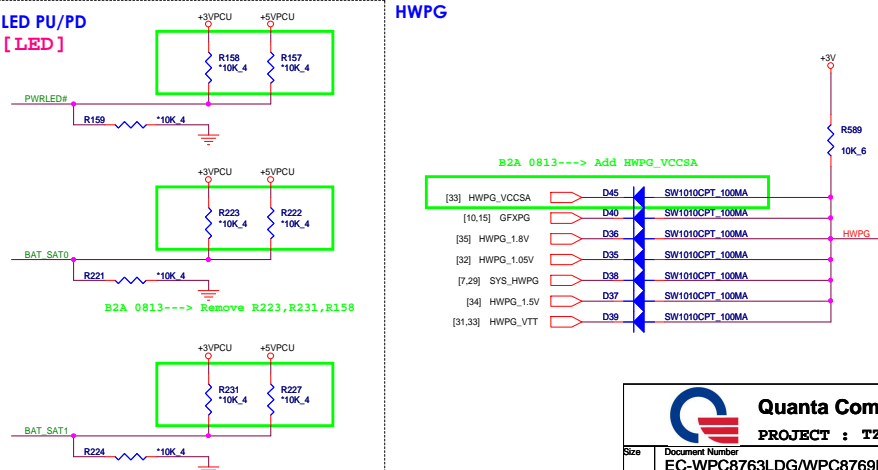
**SPI FLASH**



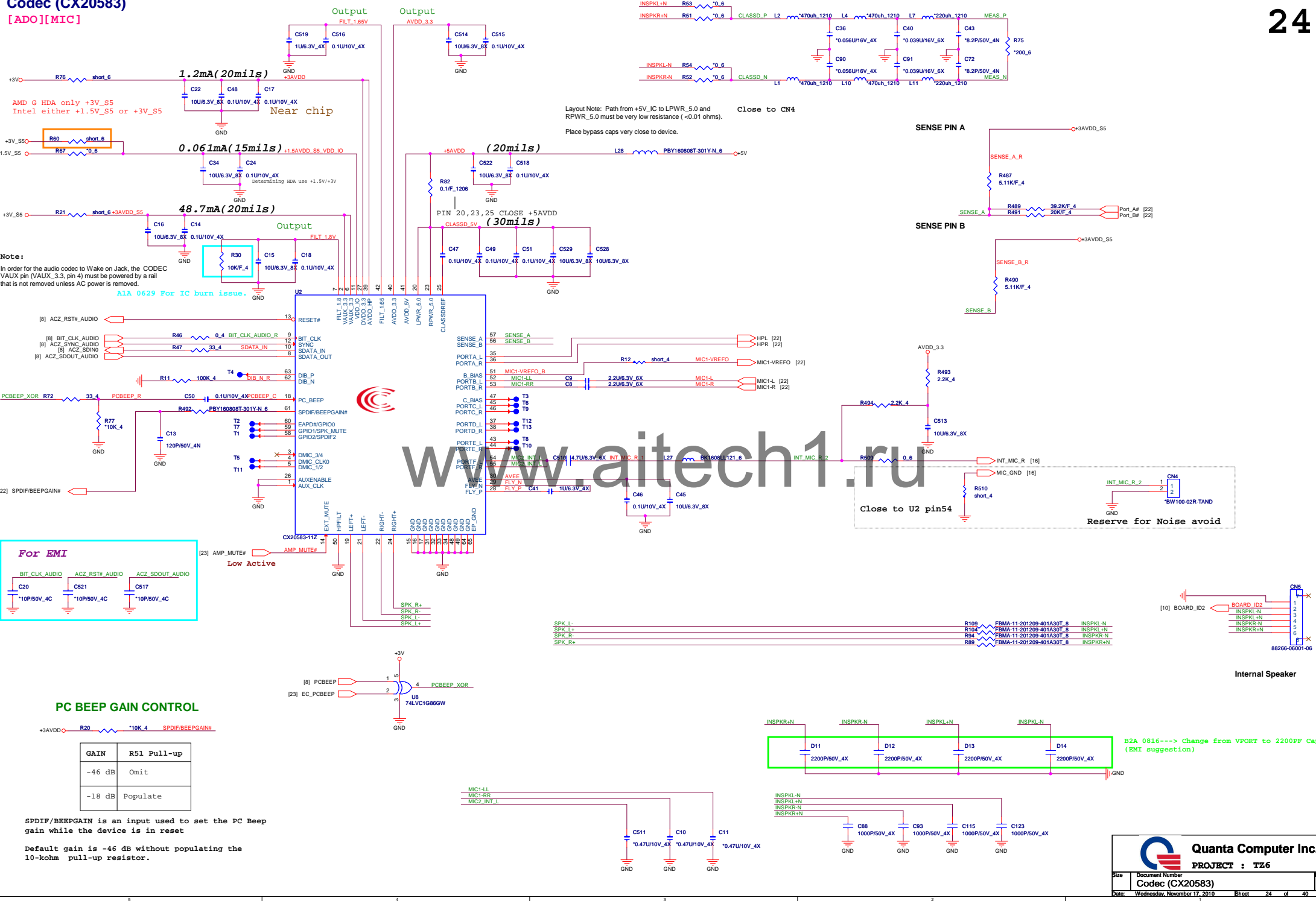
## INTERNAL KEYBOARD STRIP SET



**HWPG**



**Codec (CX20583)**  
[ADO][MIC]



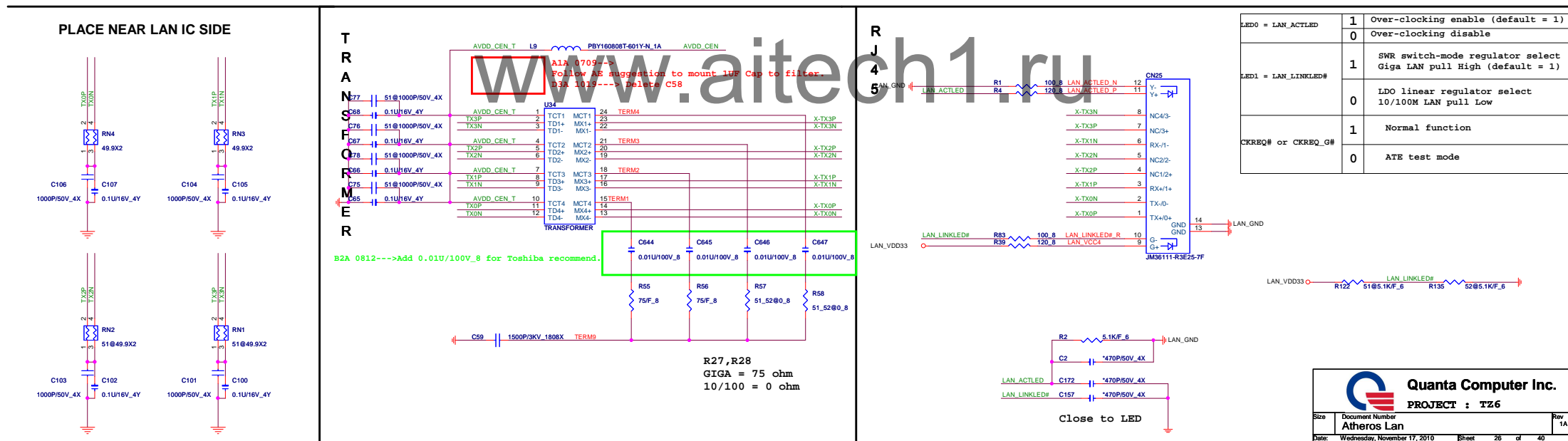
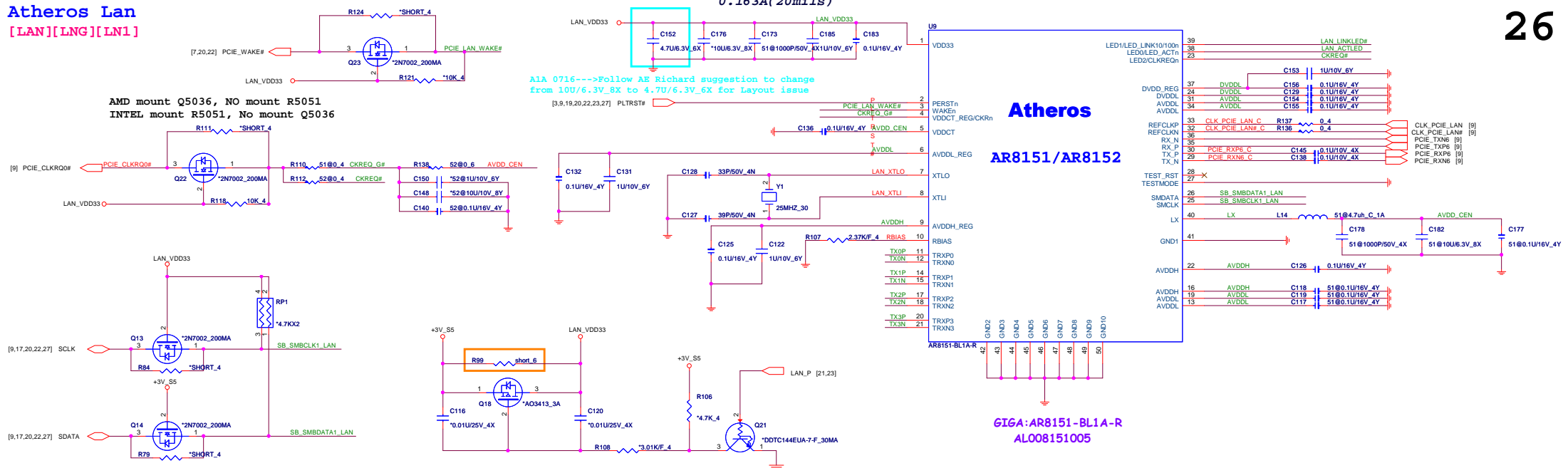
<b>GAIN</b>	<b>R51 Pull-up</b>
-46 dB	Omit
-18 dB	Populate

SPDIF/BEEPGAIN is an input used to set the PC Beep gain while the device is in reset

Default gain is -46 dB without populating the 10-kohm pull-up resistor.



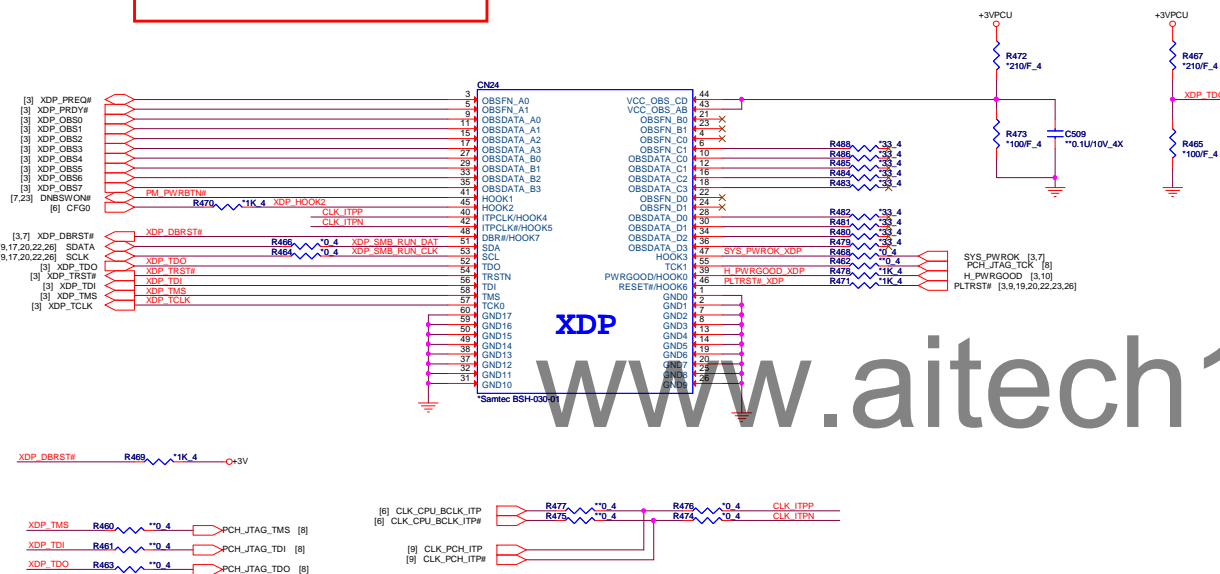




## XDP [CPU]

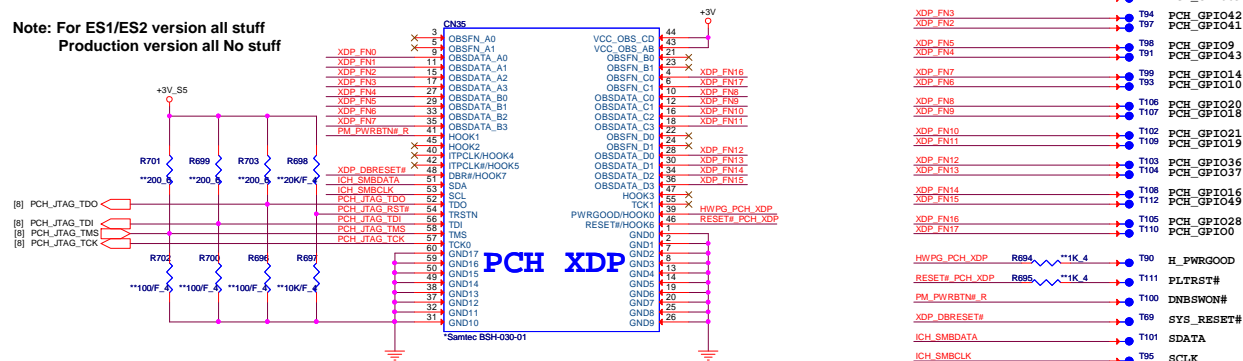
C3A 0920--->Delete CPU XDP component

+1.05V for CPU  
+3V for PCH

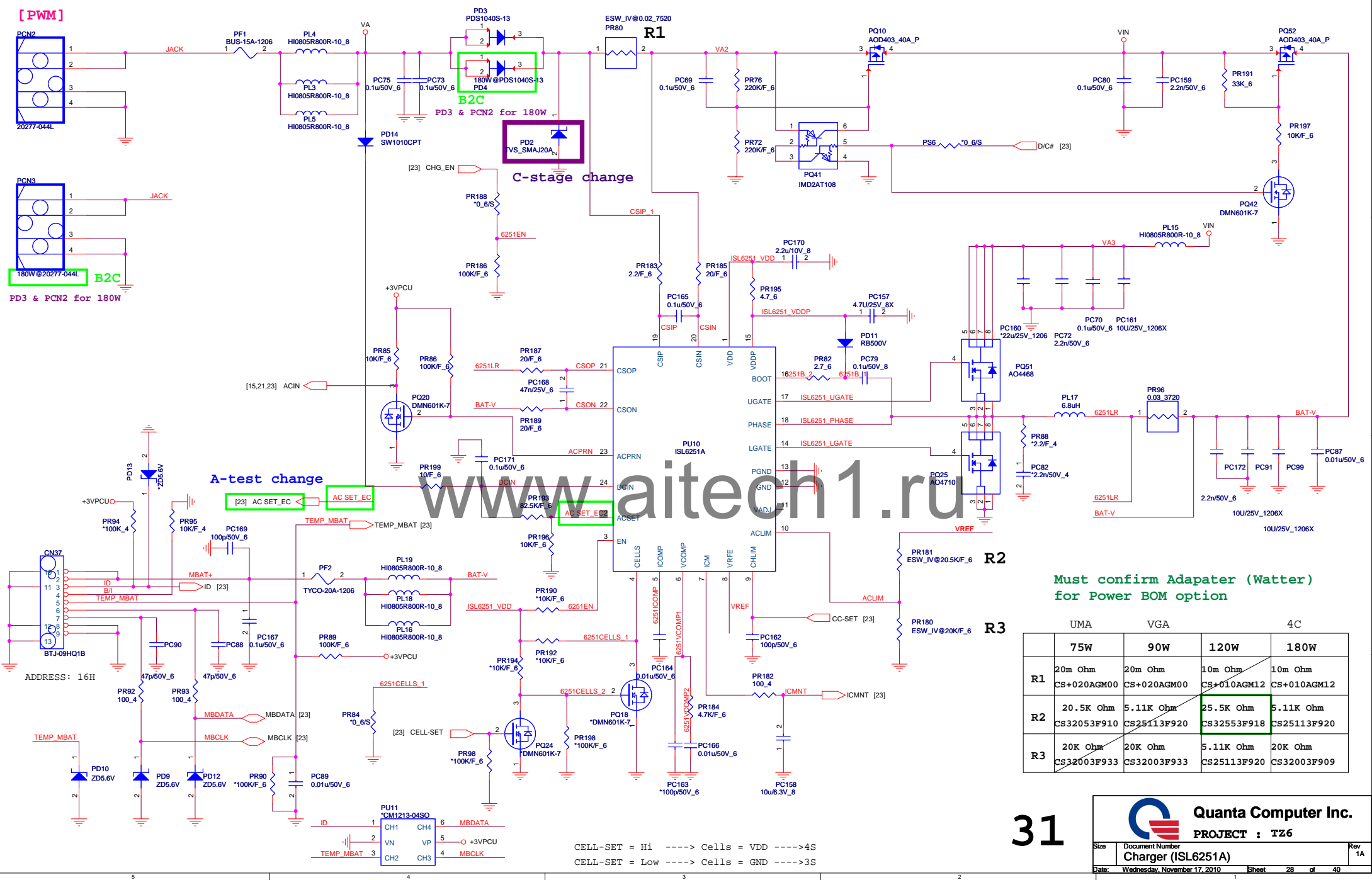


## PCH XDP [CLG]

**Note: For ES1/ES2 version all stuff**  
**Production version all No stuff**



[PWM]



Must confirm Adapter (Watter)  
for Power BOM option

	UMA	VGA	4C	
	75W	90W	120W	180W
R1	20m Ohm CS+020AGM00	20m Ohm CS+020AGM00	10m Ohm CS+010AGM12	10m Ohm CS+010AGM12
R2	20.5K Ohm CS32053F910	5.11K Ohm CS25113F920	25.5K Ohm CS32553F918	5.11K Ohm CS25113F920
R3	20K Ohm CS32003F933	20K Ohm CS32003F933	5.11K Ohm CS25113F920	20K Ohm CS32003F909

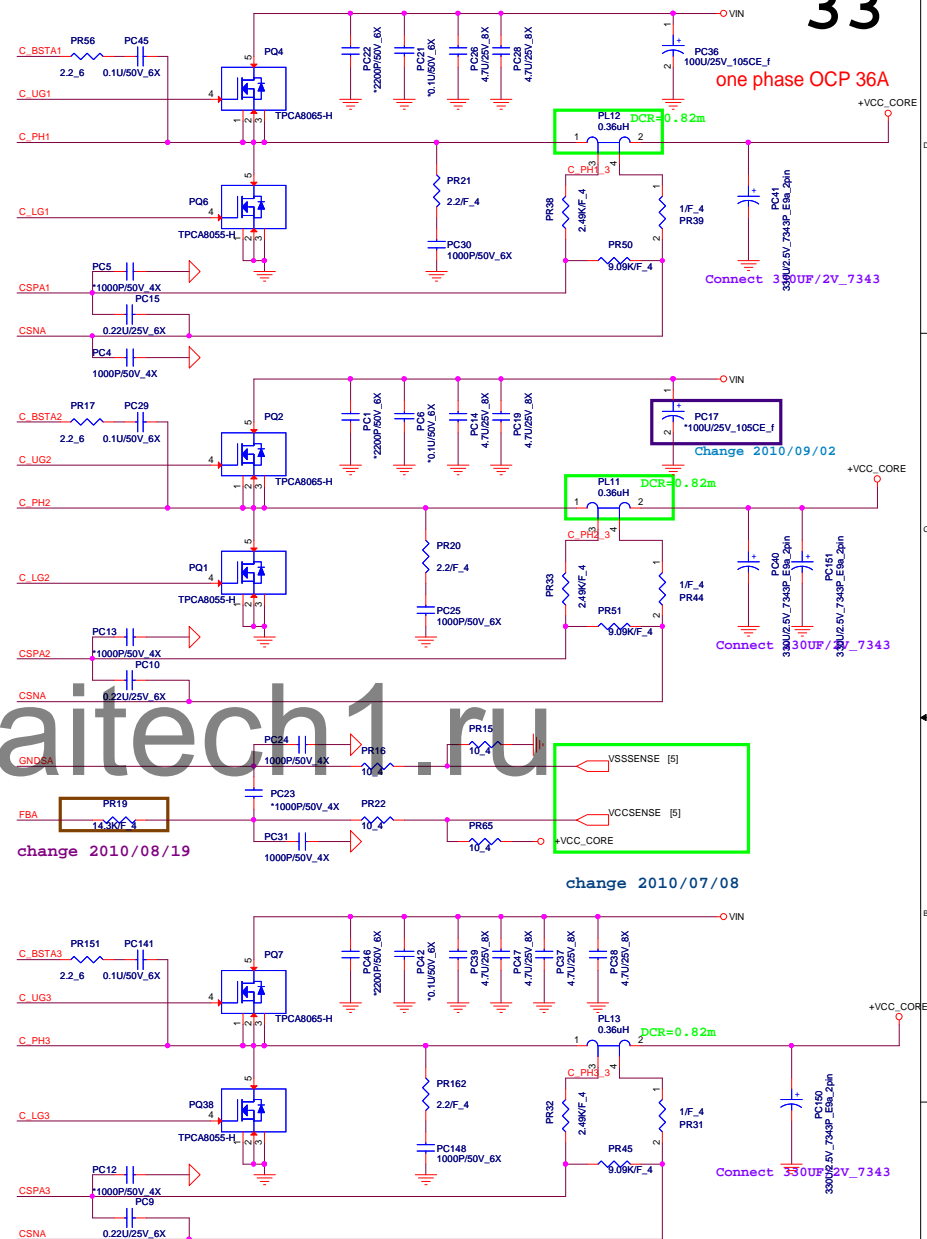
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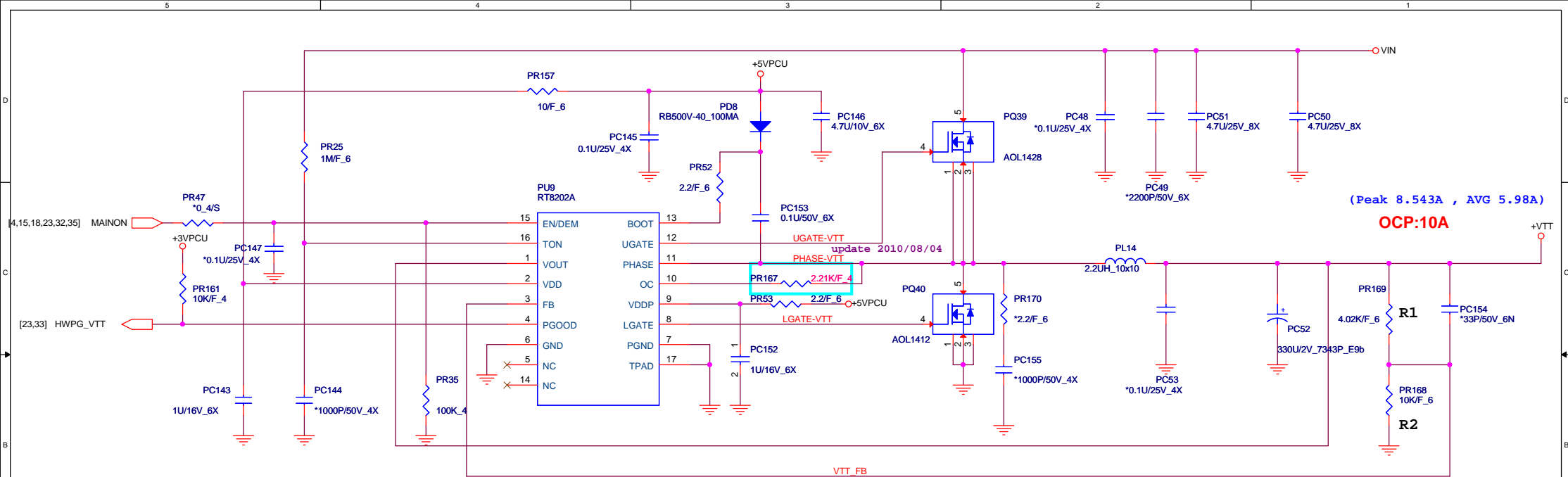
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Size	Document Number	Rev
	Charger (ISL6251A)	1A
Date:	Wednesday, November 17, 2010	Sheet 28 of 40


CELL-SET = Hi ----> Cells = VDD ---->4S  
CELL-SET = Low ----> Cells = GND ---->3S





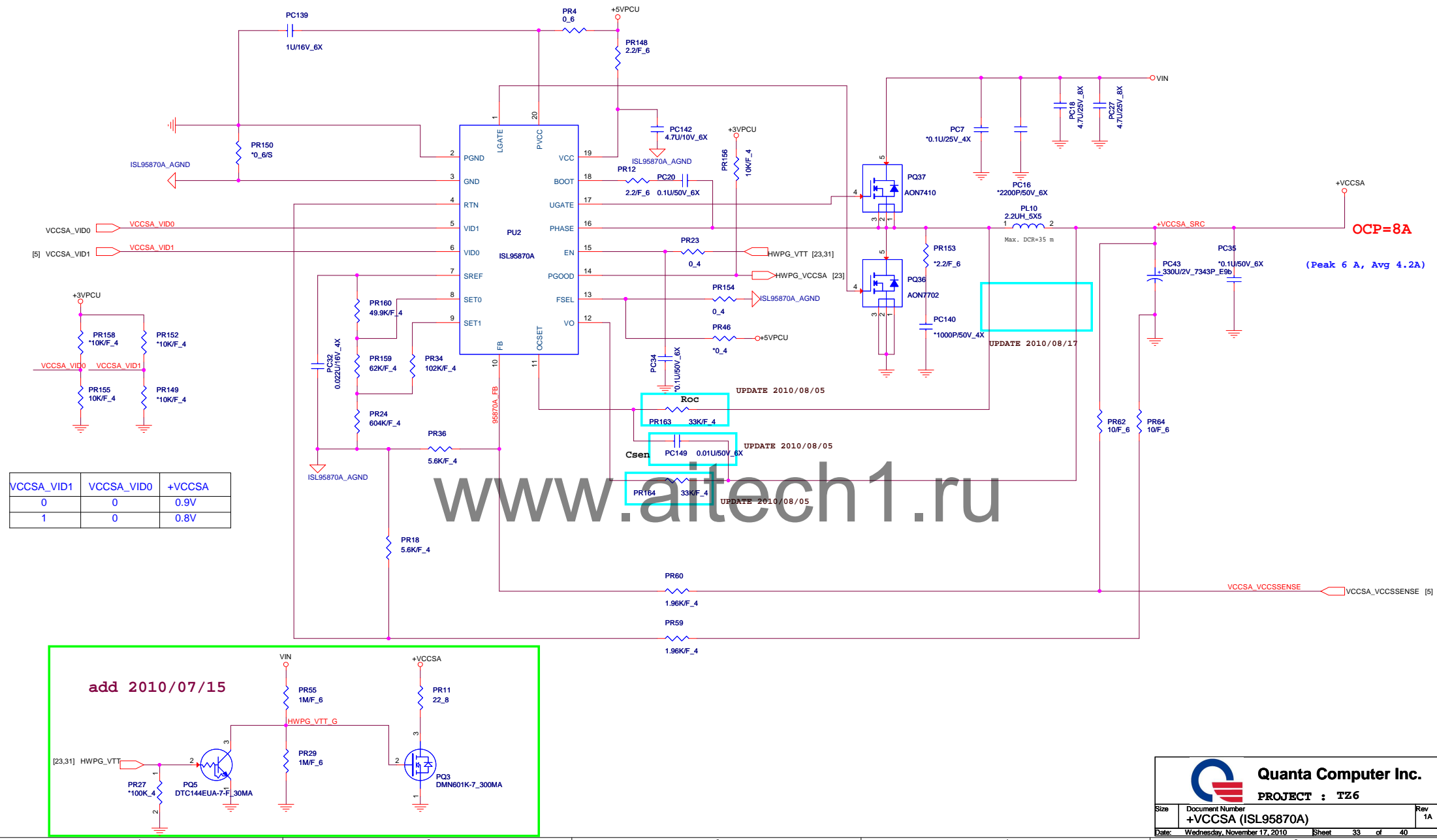


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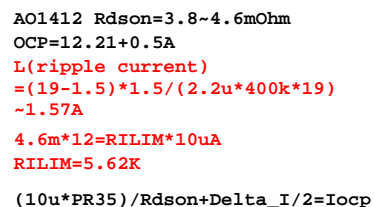
 <b>Quanta Computer Inc.</b> <b>PROJECT : TZ6</b>		Size	Document Number	Rev
			<b>+VTT (RT8202A)</b>	<b>1A</b>
Date:	Wednesday, November 17, 2010	Sheet	31	of 40

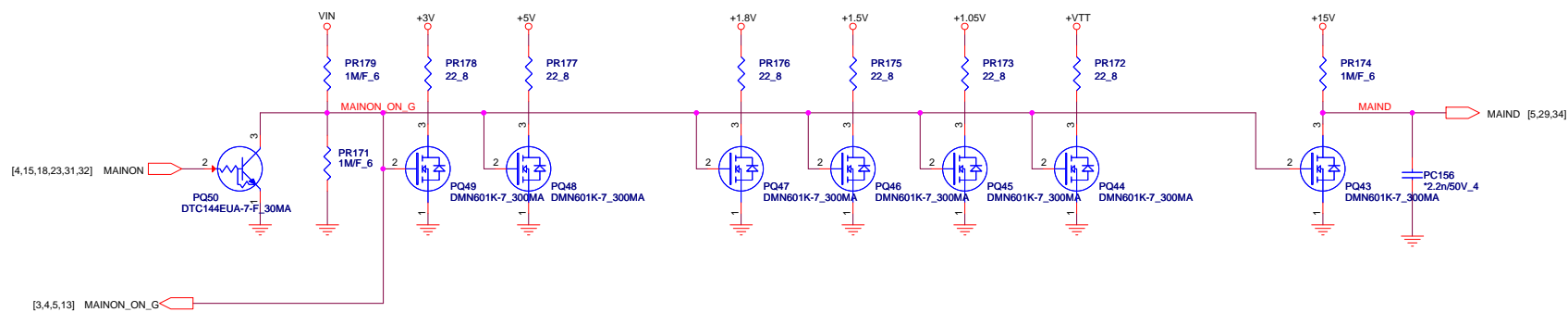






VCCSA_VID1	VCCSA_VID0	+VCCSA
0	0	0.9V
1	0	0.8V





# PCH POWER PLANE

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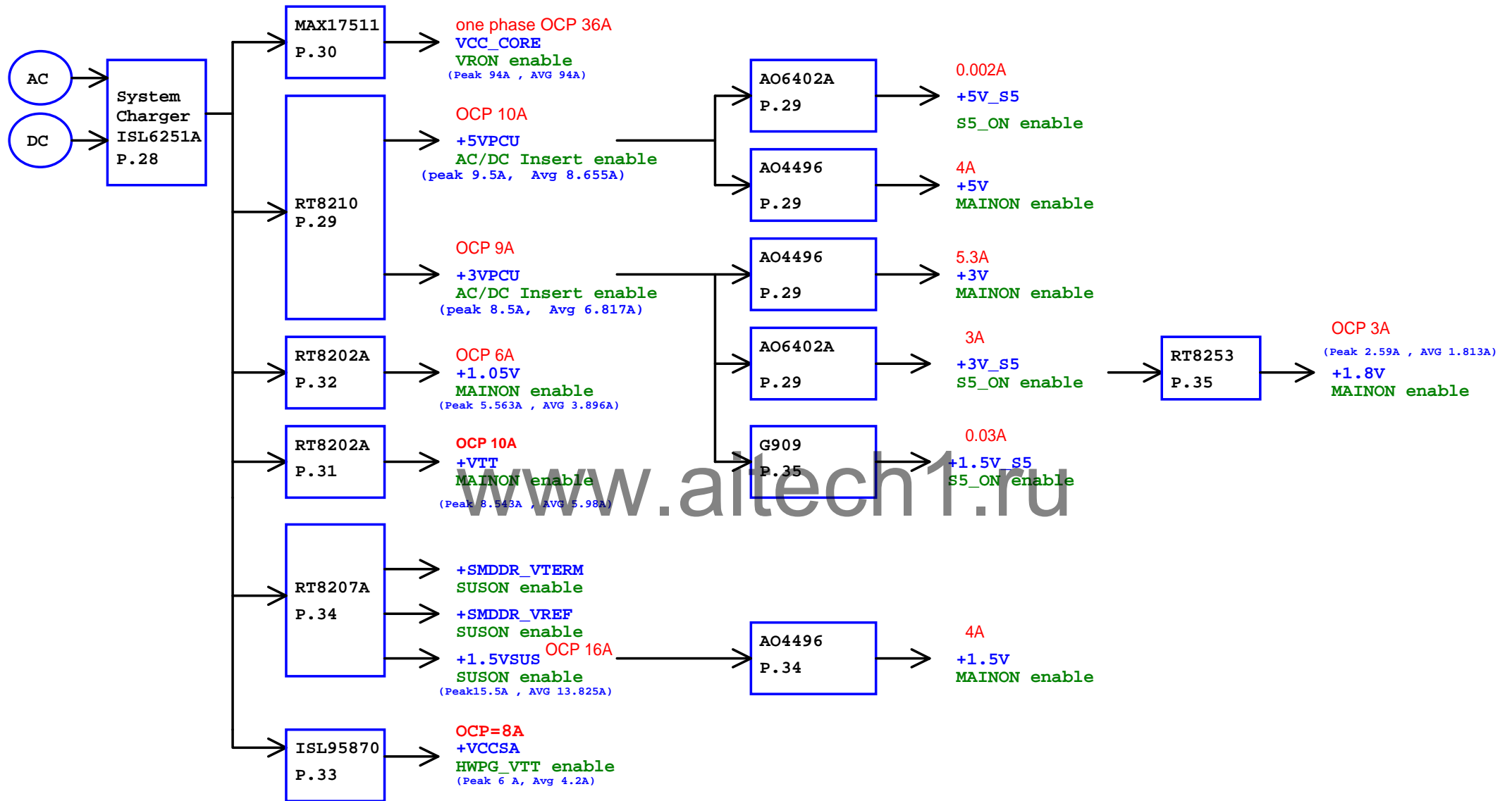
LOGIC	SUPPLY	LEVEL	S0	S3	S4	S5
Fast Flash	VccpNAND	+1.8V/+3.3V	ON	OFF	OFF	OFF
Core	DcpSusByp	+1.05V	ON	OFF	OFF	OFF
CPU	V_CPU_IO	+VTT	ON	OFF	OFF	OFF
PCI	V5REF	+5V/+3V	ON	OFF	OFF	OFF
USB	V5REF_Sus	+5V_S5/+3V_S5	ON	ON	ON	ON
DisplayPort, SATA, PCI	VCC3_3	+3V	ON	OFF	OFF	OFF
Core	VccCore	+1.05V	ON	OFF	OFF	OFF
PCIE/DMI	VccDMI	+VTT/+1.05V	ON	OFF	OFF	OFF
Fast Flash	VccME3_3	+3V	ON	OFF	OFF	OFF
PCIE/DMI,SATA,USB	VccIO	+1.05V	ON	OFF	OFF	OFF
Core	VccLAN	+1.05V	ON	OFF	OFF	OFF
Core	VccME	+1.05V	ON	OFF	OFF	OFF
RTC	VccRTC	+VCCRTC	ON	ON	ON	ON
USB&PCI	VccSus3_3	+3V_S5	ON	ON	ON	ON
IntelR HD Audio	VccSusHDA	+3V_S5	ON	ON	ON	ON
Core	VccVRM	+V1.5S_1.8S	ON	OFF	OFF	OFF
CLK	VccAClk	+1.05V	ON	OFF	OFF	OFF
CRT	VccADAC	+3V	ON	OFF	OFF	OFF
DPLL	VccADPLLA	+1.05V	ON	OFF	OFF	OFF
DPLL	VccADPLLb	+1.05V	ON	OFF	OFF	OFF
PCie/DMI	VccapIEXP	+1.05V	ON	OFF	OFF	OFF
IntelR FDI	VccFDIPLL	+1.05V	ON	OFF	OFF	OFF
SATA	VccSATAPLL	+1.05V	ON	OFF	OFF	OFF
Display	VccTX_LVDS	+1.8V	ON	OFF	OFF	OFF



Quanta Computer Inc.

PROJECT : TZ6

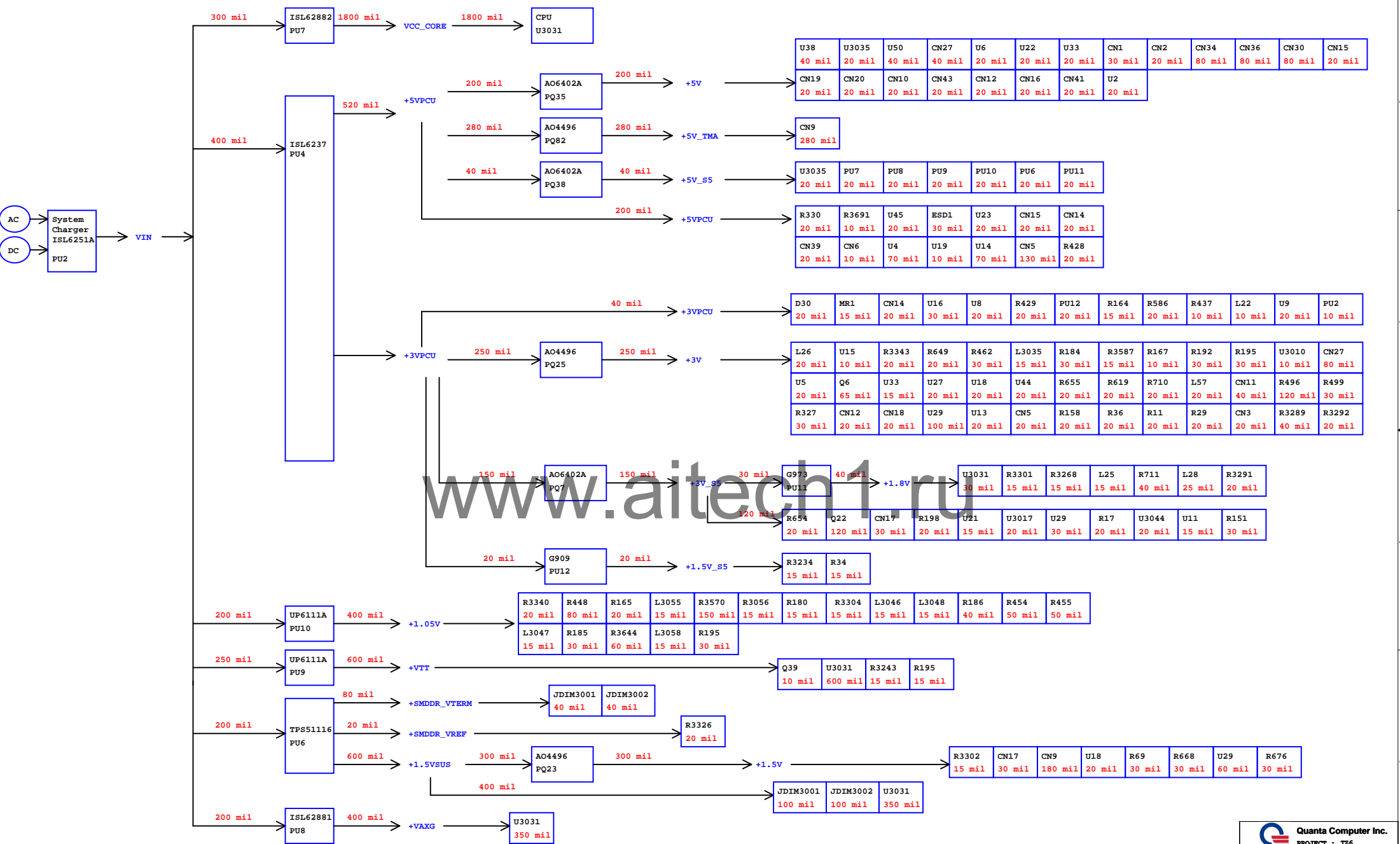
Size	Document Number	Rev
	PCH POWER PLANE	1A
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Quanta Computer Inc.

PROJECT : TZ6

Size	Document Number	Rev
	POWER TREE TABLE	1A
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Model	REV	DATE	Change List	NOTE
TZ1X	A1A	0621	Change CLG from Calpella to Huron River Change EC to 791 Remove CLK Gen Change LAN from AR8131/32 to AR8151/52 Change O2 Card Reader P/N to AJ008880011 Change SODIMM0/1 to PDC module Delete HOLE16 for N11E-GS VGA/B	
		0625		
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